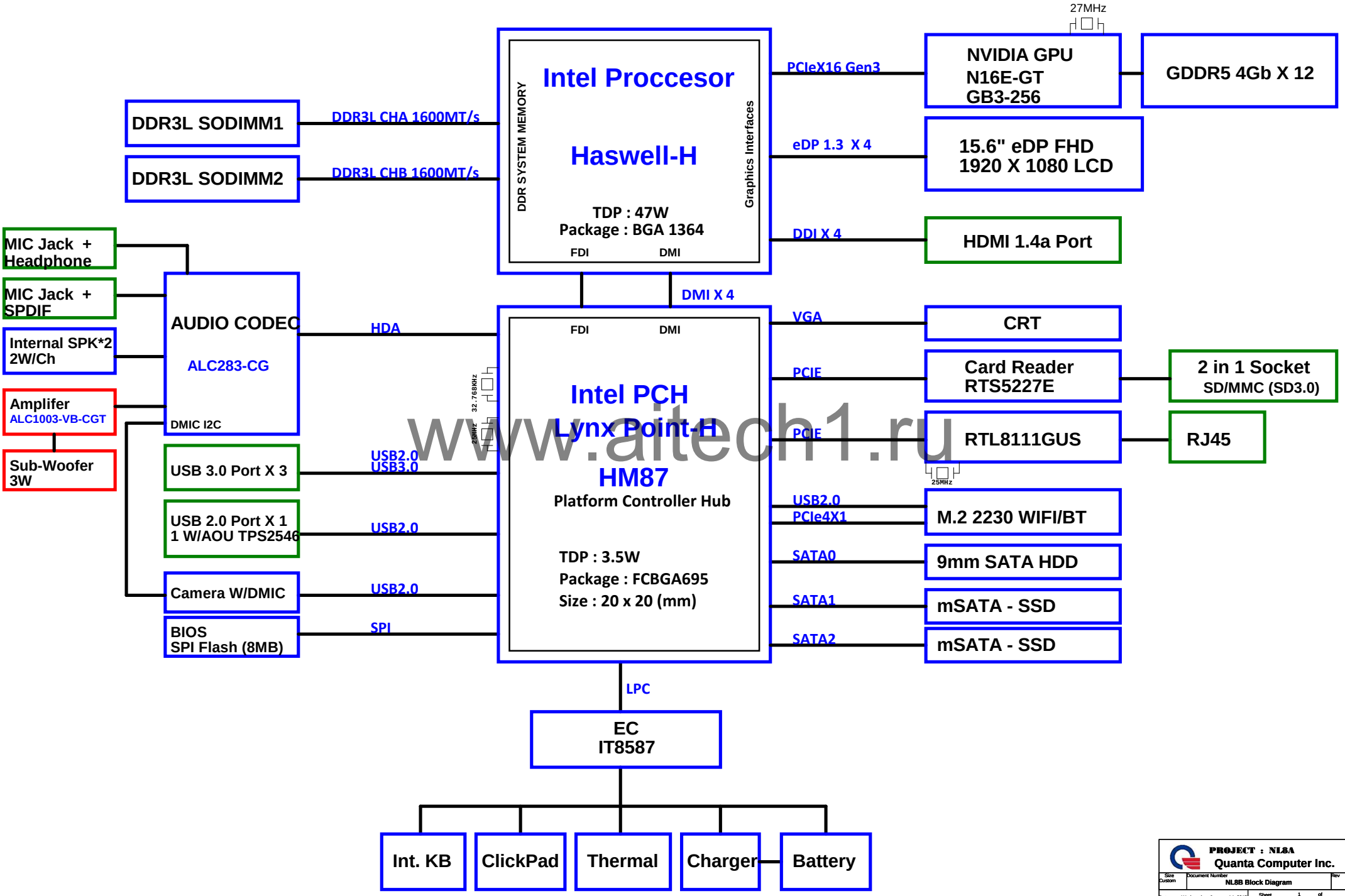
NL8B Block Diagram

01



PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NL8B Block Diagram	1A
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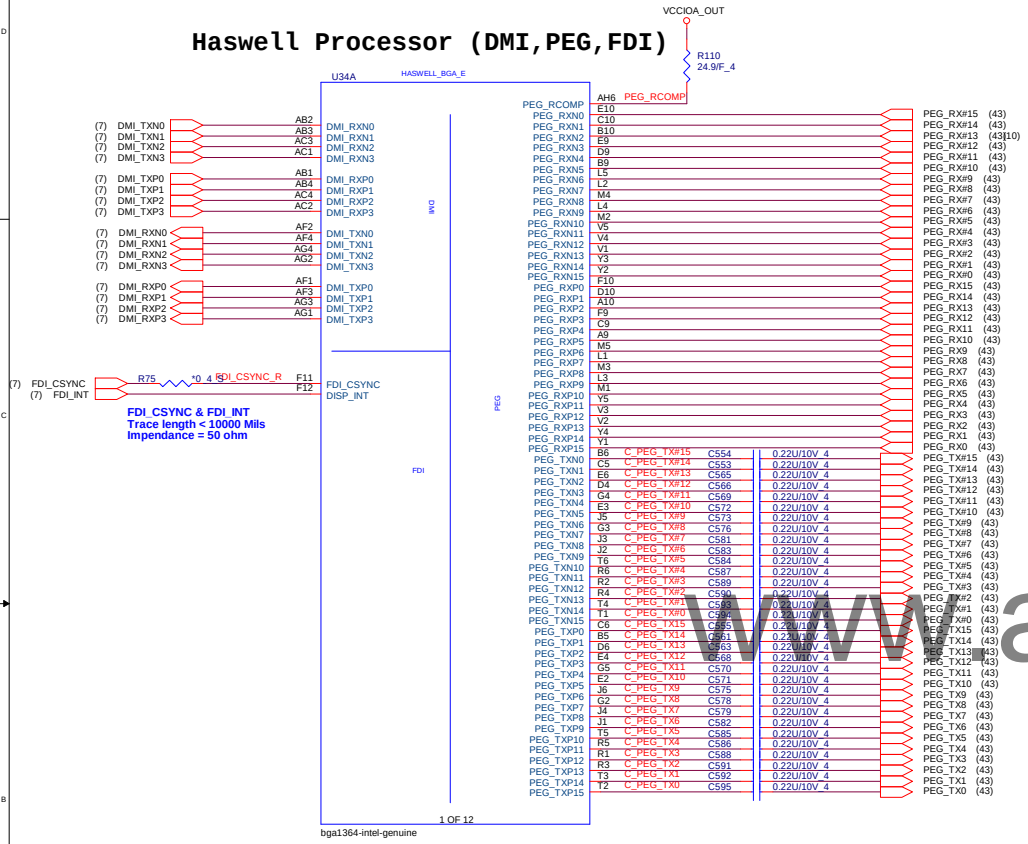
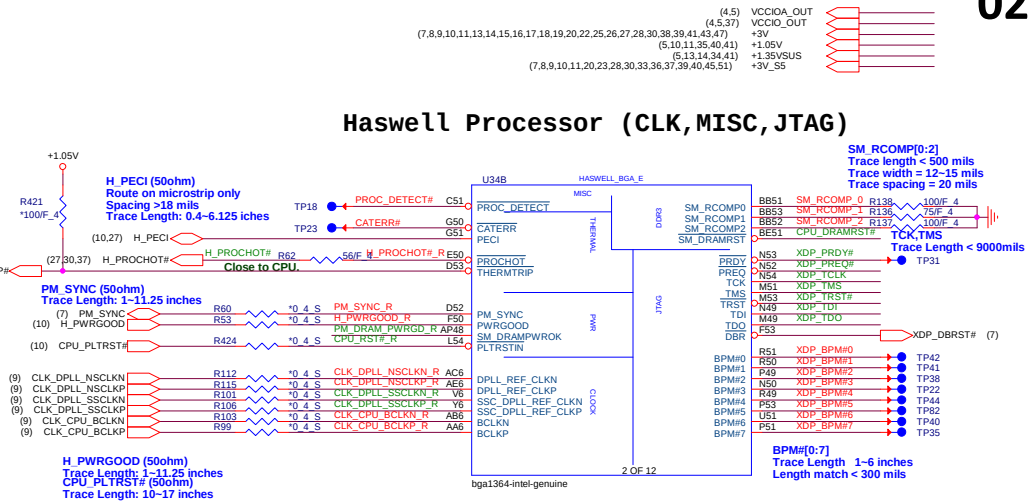
Haswell Processor (DMI,PEG,FDI)

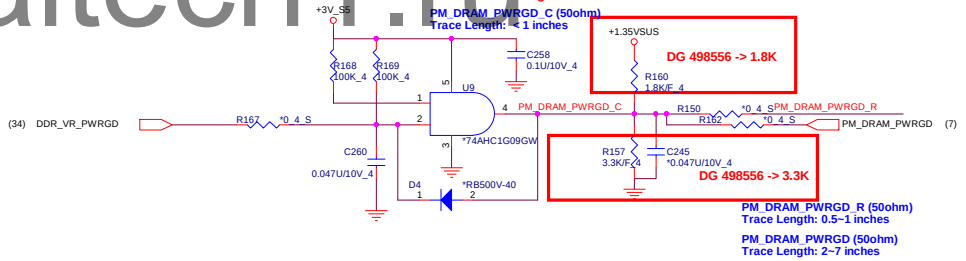


Haswell Processor (CLK,MISC,JTAG)

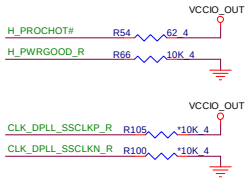


SM_DRAMPWROK Processor Input.

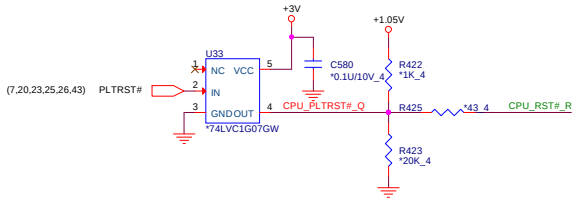
To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD



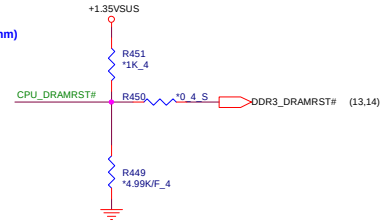
PU/PD of CPU



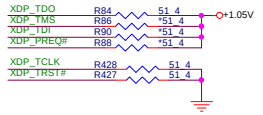
Reserved For buffer reset of PLTRSRIN#



SM_DRAMRST# Topology



XDP PU/PD



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Quanta Computer Inc.

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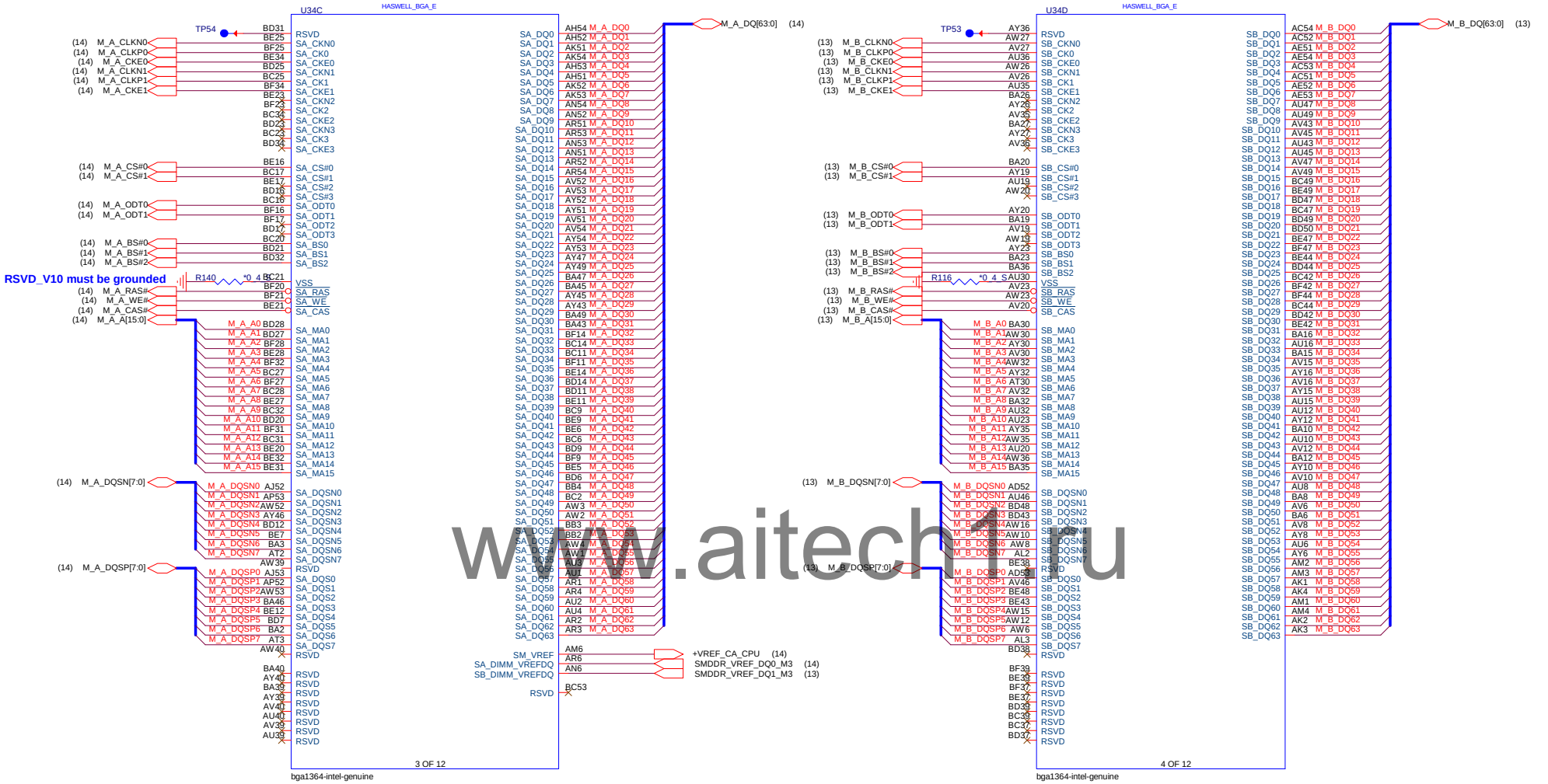
Haswell Processor (DDR3)



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Quanta Computer Inc.		
Size: Custom	Document Number: Haswell 2/5 (DDR3 I/F)	Rev: 3B
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Haswell Processor (DDI,eDP,FDI)

04

(2,5) VCCIOA_OUT
(2,5,37) VCCIO_OUT

U34J HASWELL_BGA_E

HDMI

(17) HDMI_TX2- C25 DDIB_TXN0
(17) HDMI_TX2+ D25 DDIB_TXP0
(17) HDMI_TX1- A25 DDIB_TXN1
(17) HDMI_TX1+ B25 DDIB_TXP1
(17) HDMI_TX0- C24 DDIB_TXN2
(17) HDMI_TX0+ D24 DDIB_TXP2
(17) HDMI_CLK- A24 DDIB_TXN3
(17) HDMI_CLK+ B24 DDIB_TXP3

C21 DDIC_TXN0
D21 DDIC_TXP0
A21 DDIC_TXN1
B21 DDIC_TXP1
C20 DDIC_TXN2
D20 DDIC_TXP2
A20 DDIC_TXN3
B20 DDIC_TXP3

C16 DDID_TXN2
D16 DDID_TXP2
A16 DDID_TXN3
B16 DDID_TXP3

C17 DDID_TXN0
D17 DDID_TXP0
A17 DDID_TXN1
B17 DDID_TXP1

EDP_AUXN F15 EDP_AUXN (15)
EDP_AUXP F14 EDP_AUXP (15)
EDP_HPD E14 EDP_HPD_Q

EDP_TXN0 C14 EDP_TXN0 (15)
EDP_TXN1 A12 EDP_TXN1 (15)
EDP_TXP0 D14 EDP_TXP0 (15)
EDP_TXP1 B12 EDP_TXP1 (15)

EDP_RCOMP AG6 EDP_RCOMP R108 24.9/F_4 VCCIOA_OUT
EDP_DISP_UTIL E12

FDI_TXN0 C12 FDI_TXN0 (7)
FDI_TXP0 D12 FDI_TXP0 (7)
FDI_TXN1 A14 FDI_TXN1 (7)
FDI_TXP1 B14 FDI_TXP1 (7)

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eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils

VCCIO_OUT
R64 10K_4
EDP_HPD_Q
Q3 2N7002K
R50 100K_4
EDP_HPD (15)

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Custom	Haswell 3/5 (DDI/eDP)	3B
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Haswell Processor (POWER)

(2,13,14,34,41) +1.35VSUS
(6,37,41) +VCC_CORE
(2,4,37) VCCIO_OUT
(2,10,11,35,40,41) +1.05V
(2,4) VCCIOA_OUT

+1.35VSUS
4.2A

C145 22U/6.3V_6, C143 22U/6.3V_6, C141 *22U/6.3V_6, C140 *22U/6.3V_6, C138 *22U/6.3V_6, C147 *22U/6.3V_6
C137 *22U/6.3V_6, C144 *22U/6.3V_6, C142 *22U/6.3V_6, C139 *22U/6.3V_6, C146 *22U/6.3V_6
C215 10U/6.3V_6, C214 10U/6.3V_6, C223 *10U/6.3V_6, C221 *10U/6.3V_6, C216 *10U/6.3V_6
C218 *10U/6.3V_6, C217 *10U/6.3V_6, C226 *10U/6.3V_6, C220 *10U/6.3V_6, C219 *10U/6.3V_6

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

U34E HASWELL_BGA_E

J17 RSVD, J21 RSVD, J26 RSVD, J31 RSVD
AR29 VDDQ, AR31 VDDQ, AR33 VDDQ, AT13 VDDQ, AT19 VDDQ, AT23 VDDQ, AT27 VDDQ, AT32 VDDQ, AT36 VDDQ, AV37 VDDQ, AW22 VDDQ, AW25 VDDQ, AW29 VDDQ, AW33 VDDQ, AY18 VDDQ, BB21 VDDQ, BB22 VDDQ, BB26 VDDQ, BB27 VDDQ, BB30 VDDQ, BB31 VDDQ, BB34 VDDQ, BB36 VDDQ, BD22 VDDQ, BD26 VDDQ, BD30 VDDQ, BD33 VDDQ, BE18 VDDQ, BE22 VDDQ, BE26 VDDQ, BE30 VDDQ, BE33 VDDQ

TP47 AN31 RSVD, +VCC_CORE L6 VCC, M6 VCC, TP50 AN22 RSVD, TP51 AN18 RSVD

+VCC_CORE R68 100_4
(37) VCC_SENSE R56 *0_4_S — VCC_SENSE_R — C50 VCC_SENSE, AH9 RSVD
300mA VCCIO_OUT R47 *0_8_S — +VCCIO_OUT_R — D51 VCCIO_OUT
+1.05V R63 *0_8 — +VCCIO_PCH_R — F17 FC_F17
300mA VCCIOA_OUT R113 *0_8_S — +VCCIOA_OUT_R — AK6 VCOMP_OUT
TP48 AN33 RSVD, TP45 W9 RSVD, TP30 J12 RSVD, TP52 AR49 RSVD

H_CPU_SVIDART# J53 VIDALERT
H_CPU_SVIDCLK J52 VIDSCLK
H_CPU_SVIDDAT J50 VIDSOUT

TP10 PWR_DEBUG_R — R65 *0_4_S — B51 VSS, F19 PWR_DEBUG
E52 VSS, V49 RSVD_TP, U49 RSVD_TP, AM49 RSVD_TP, W49 RSVD_TP, V50 RSVD_TP
TP43, TP39, TP49, TP46
AN49 VSS, AJ49 VSS, AC50 VSS, AK49 VSS, AJ50 VSS, AP49 VSS, AB50 VSS, AP50 VSS, AD50 VSS, AM50 VSS

+VCC_CORE A36 VCC, A38 VCC, A39 VCC, A42 VCC, A43 VCC, A45 VCC, A46 VCC, A48 VCC, AA46 VCC, AA47 VCC, AA8 VCC, AA9 VCC

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B43 VCC
B45 VCC, B46 VCC, B48 VCC, C27 VCC, C28 VCC, C31 VCC, C32 VCC, C34 VCC, C36 VCC, C38 VCC, C39 VCC, C42 VCC, C43 VCC, C45 VCC, C46 VCC, C48 VCC, D27 VCC, D28 VCC, D31 VCC, D32 VCC, D34 VCC, D36 VCC, D38 VCC, D39 VCC, D42 VCC, D43 VCC, D45 VCC, D46 VCC, D48 VCC, E27 VCC, E28 VCC, E31 VCC, E32 VCC, E34 VCC, E36 VCC, E38 VCC, E39 VCC, E42 VCC, E43 VCC, E45 VCC, E46 VCC, E48 VCC, F27 VCC, F28 VCC, F31 VCC, F32 VCC, F34 VCC, F36 VCC, F38 VCC, F39 VCC, F42 VCC, F43 VCC, F45 VCC, F46 VCC, F48 VCC, G27 VCC, G29 VCC, G31 VCC, G32 VCC, G34 VCC, G36 VCC, G38 VCC, G39 VCC, G42 VCC, G43 VCC, G45 VCC, G46 VCC, G48 VCC, H11 VCC, H12 VCC, H13 VCC, H14 VCC, H16 VCC, H17 VCC, H18 VCC, H19 VCC, H20 VCC, H21 VCC, H23 VCC, H24 VCC, H25 VCC, H26 VCC, H27 VCC, H29 VCC

FC_D5 D5, FC_D3 D3

VCC_CORE 85A
+VCC_CORE
C80 22U/6.3V_6, C79 22U/6.3V_6, C78 22U/6.3V_6, C77 22U/6.3V_6, C89 22U/6.3V_6, C63 22U/6.3V_6
C558 22U/6.3V_6, C86 22U/6.3V_6, C82 22U/6.3V_6, C74 22U/6.3V_6, C68 22U/6.3V_6, C69 22U/6.3V_6
C52 22U/6.3V_6, C557 22U/6.3V_6, C90 22U/6.3V_6, C54 22U/6.3V_6, C67 22U/6.3V_6, C85 22U/6.3V_6
C53 22U/6.3V_6, C55 10U/6.3V_6, C81 10U/6.3V_6, C556 10U/6.3V_6, C559 10U/6.3V_6, C73 10U/6.3V_6
C66 10U/6.3V_6, C72 10U/6.3V_6, C71 10U/6.3V_6, C65 10U/6.3V_6, C64 10U/6.3V_6, C70 10U/6.3V_6

VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

+1.05V — R946 *0_6 — C1084 *0.1U/10V_4
R947 *6.04K/F_4 — EC_PWROK_R (7)
R948 *2.67K/F_4
EC-D-23

Power Test Propose

+1.05V — R61 150_4 — PWR_DEBUG_R — R78 *10K_4
MOW WW12-->if PWR_DEBUG# is routed to the XDP the R741 value is 150 ohm

+1.05V — R48 *0_8 — VCCIO_OUT — C48 *4.7U/6.3V_6

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

VCCIO_OUT
Place PU resistor close to CPU — R73 130/F_4
H_CPU_SVIDDAT — R57 *0_4_S — VR_SVIDDAT (37)
VCCIO_OUT
Place PU resistor close to CPU — R58 75/F_4
H_CPU_SVIDART# — R74 43_4 — VR_SVIDART# (37)
H_CPU_SVIDCLK — R59 *0_4_S — VR_SVIDCLK (37)

+VCC_CORE

U34F HASWELL_BGA_E

AB45 VCC, AB46 VCC, AB8 VCC, AC46 VCC, AC47 VCC, AC8 VCC, AC9 VCC, AD46 VCC, AD8 VCC, AE46 VCC, AE47 VCC, AE8 VCC, AF8 VCC, AG46 VCC, AG8 VCC, AH46 VCC, AH47 VCC, AH8 VCC, AJ45 VCC, AJ46 VCC, AK46 VCC, AK47 VCC, AK8 VCC, AL45 VCC, AL46 VCC, AL8 VCC, AL9 VCC, AM46 VCC, AM47 VCC, AM8 VCC, AM9 VCC, AN10 VCC, AN12 VCC, AN13 VCC, AN14 VCC, AN15 VCC, AN16 VCC, AN17 VCC, AN19 VCC, AN20 VCC, AN21 VCC, AN23 VCC, AN24 VCC, AN25 VCC, AN26 VCC, AN27 VCC, AN29 VCC, AN30 VCC, AN32 VCC, AN34 VCC, AN36 VCC, AN38 VCC, AN39 VCC, AN40 VCC, AN41 VCC, AN42 VCC, AN43 VCC, AN44 VCC, AN45 VCC, AN46 VCC, AN8 VCC, AN9 VCC, AP10 VCC, AP12 VCC, AP13 VCC, AP14 VCC, AP15 VCC, AP16 VCC, AP17 VCC, AP18 VCC, AP19 VCC, AP20 VCC, AP21 VCC, AP22 VCC, AP23 VCC, AP24 VCC, AP25 VCC, AP26 VCC, AP27 VCC, AP29 VCC, AP30 VCC, AP31 VCC, AP32 VCC, AP33 VCC, AP34 VCC, AP35 VCC, AP36 VCC, AP37 VCC, AP38 VCC, AP39 VCC, AP40 VCC, AP41 VCC, AP42 VCC, AP43 VCC, AP44 VCC, AP46 VCC, AP47 VCC, AP8 VCC, AP9 VCC, AR35 VCC, AR37 VCC, AR39 VCC, AR41 VCC, AR43 VCC, AR45 VCC, AR46 VCC, H30 VCC, H31 VCC, H32 VCC
H33 VCC, H34 VCC, H36 VCC, H37 VCC, H38 VCC, H39 VCC, H40 VCC, H42 VCC, H43 VCC, H45 VCC, H46 VCC, H48 VCC, H8 VCC, H9 VCC, J10 VCC, J14 VCC, J19 VCC, J24 VCC, J29 VCC, J33 VCC, J36 VCC, J37 VCC, J38 VCC, J39 VCC, J40 VCC, J42 VCC, J43 VCC, J45 VCC, J46 VCC, J48 VCC, J8 VCC, J9 VCC, K38 VCC, K40 VCC, K43 VCC, K44 VCC, K45 VCC, K46 VCC, K48 VCC, K8 VCC, K9 VCC, L37 VCC, L38 VCC, L39 VCC, L40 VCC, L42 VCC, L43 VCC, L44 VCC, L46 VCC, L47 VCC, L8 VCC, M37 VCC, M38 VCC, M39 VCC, M40 VCC, M42 VCC, M43 VCC, M44 VCC, M45 VCC, M46 VCC, M8 VCC, M9 VCC, N37 VCC, N38 VCC, N39 VCC, N40 VCC, N42 VCC, N43 VCC, N44 VCC, N46 VCC, N47 VCC, N8 VCC, N9 VCC, P45 VCC, P46 VCC, P8 VCC, R46 VCC, R47 VCC, R8 VCC, R9 VCC, T45 VCC, T46 VCC, U46 VCC, U47 VCC, U8 VCC, U9 VCC, V45 VCC, V46 VCC, V8 VCC, W46 VCC, W47 VCC, W8 VCC, Y45 VCC, Y46 VCC, Y8 VCC, A27 VCC, A28 VCC, A31 VCC, A32 VCC, A34 VCC, B27 VCC, B28 VCC, B31 VCC, B32 VCC, B34 VCC, B36 VCC, B38 VCC, B39 VCC, B42 VCC

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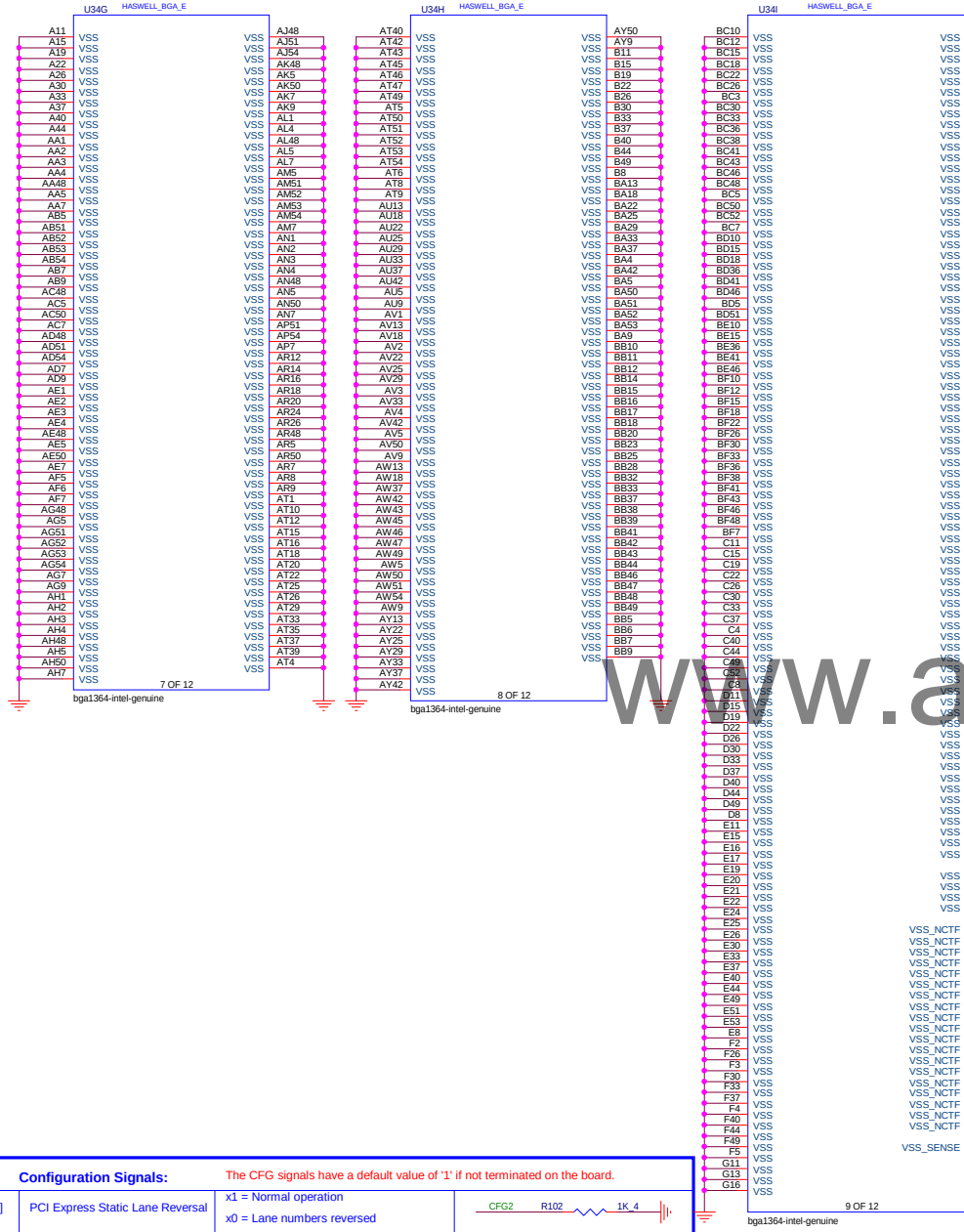
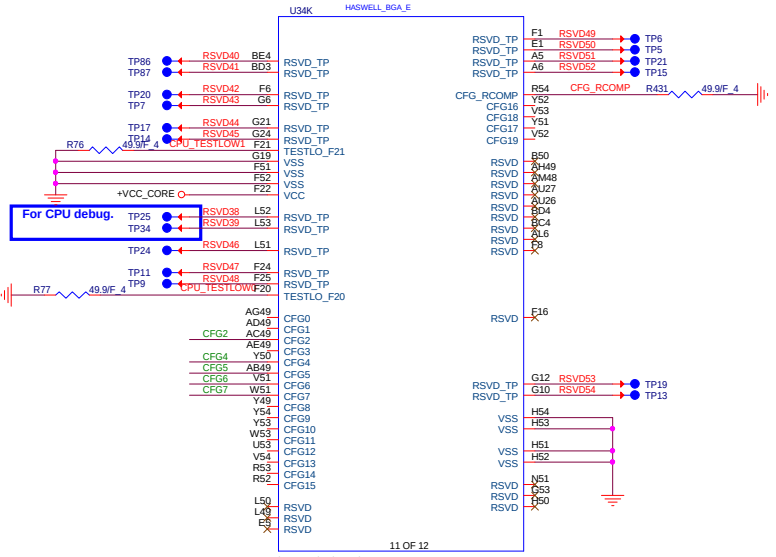
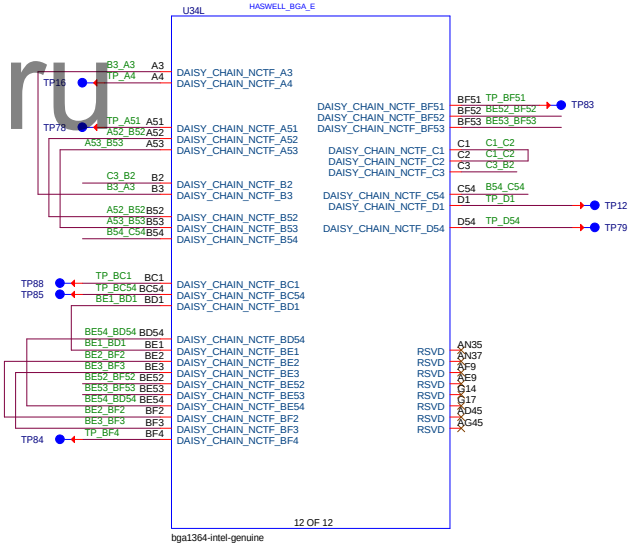
Haswell Processor (GND)

Haswell Processor (CFG,RSVD)

06







Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R102 1K_4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R95 1K_4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R91 *1K_4 CFG5 R96 *1K_4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	CFG7 R93 *1K_4

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(8,9,11,17,18,23,36,41) +1.5V
(2,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,41,43,47) +3V
(2,8,9,10,11,20,23,28,30,33,36,37,39,40,45,51) +3V_S5

Lynx Point (DMI,FDI,PM)

U40B LPT_PCH_M_EDS REV = 5

DMI_RXN_0 AW22 ← (2) DMI_RXN0
DMI_RXN_1 AR20 ← (2) DMI_RXN1
DMI_RXN_2 AP17 ← (2) DMI_RXN2
DMI_RXN_3 AV20 ← (2) DMI_RXN3
DMI_RXP_0 AY22 ← (2) DMI_RXP0
DMI_RXP_1 AP20 ← (2) DMI_RXP1
DMI_RXP_2 AR17 ← (2) DMI_RXP2
DMI_RXP_3 AW20 ← (2) DMI_RXP3
DMI_TXN_0 BD21 → (2) DMI_TXN0
DMI_TXN_1 BE20 → (2) DMI_TXN1
DMI_TXN_2 BD17 → (2) DMI_TXN2
DMI_TXN_3 BE18 → (2) DMI_TXN3
DMI_TXP_0 BB21 → (2) DMI_TXP0
DMI_TXP_1 BC20 → (2) DMI_TXP1
DMI_TXP_2 BB17 → (2) DMI_TXP2
DMI_TXP_3 BC18 → (2) DMI_TXP3
DMI_IREF BE16 ← R531 *0_4_S ← +1.5V
TP12 AW17
TP7 AV17
DMI_RCOMP AY17 ← R222 7.5K/F_4

FDI_RXN_0 AJ35 → FDI_TXN0 (4)
FDI_RXN_1 AL35 → FDI_TXN1 (4)
FDI_RXP_0 AJ36 → FDI_TXP0 (4)
FDI_RXP_1 AL36 → FDI_TXP1 (4)
TP16 AV43
TP5 AY45
TP15 AV45
TP10 AW44
FDI_CSYNC AL39 → FDI_CSYNC (2)
FDI_INT AL40 → FDI_INT (2)
FDI_IREF AT45 → R507 *0_4_S → +1.5V
TP17 AU42
TP13 AU44
FDI_RCOMP AR44 → R508 7.5K/F_4

SUSACK# R6 ← for DS3 R626 *0_4_S ← SUSACK#_R ← (27) SUSACK#EC
SYS_RESET# AM1 ← R304 *0_4_S ← SYS_RESET# ← (2) XDP_DBRST#
SYS_PWROK AD7 ← R268 *0_4_S ← SYS_PWROK_R ← SYS_PWROK
PWROK F10 ← EC_PWROK_R ← (5) EC_PWROK_R
EC-D-23
APWROK AB7 ← APWROK
DRAMPWROK H3 ← (2) PM_DRAM_PWRGD
RSMRST# J2 ← R317 *0_4_S ← PCH_RSMRST# ← (27) RSMRST#
SUSWARN#/SUSPWRNACK/GPIO30 J4 ← for DS3 R624 *0_4_S ← PCH_SUSPWRACK ← (27) SUSWARN#EC
PWRBTN# K1 ← for DS3 R583 *0_4_S ← PCH_PWRBTN# ← (27) SIO_PWRBTN#
ACPRESENT/GPIO31 E6 ← for DS3 R281 *0_4_S ← PCH_ACPRESENT ← (27,45) AC_PRESENT
EC-B-05
BATLOW#/GPIO72 K7 ← PCH_BATLOW#
RI# N4 ← PCH_RI#
TP21 AB10 → TP65
SLP_WLAN#/GPIO29 D2 ← WLAN_AOAC_ON ← (23) WLAN_AOAC_ON

DSWVRMEN C8 → DSWVREN (8)
DPWROK L13 ← DPWROK_R
WAKE# K3 ← PCIE_WAKE# → PCIE_WAKE# (20,23)
CLKRUN# AN7 ← CLKRUN# → CLKRUN# (27)
(SUS) SUS_STAT#/GPIO61 U7 → SUS_STAT# → TP66
(SUS) SUSCLK/GPIO62 Y6 → SUSCLK (8)
(SUS) SLP_S5#/GPIO63 Y7 → TP64
SLP_S4# C6 → R600 *0_4_S → SLP_S4# (27)
SLP_S3# H1 → R584 *0_4_S → SLP_S3# (27)
SLP_A# F3
SLP_SUS# F1 → for DS3 R585 *0_4_S → SLP_SUS# (27)
PMSYNCH AY3 ← PCH_SYNCH ← R569 *0_4_S ← PM_SYNC (2)
SLP_LAN# G5

System Power Management

LPT_PCH_M_EDS/BGA 4 OF 11

Lynx Point (CRT,PCI,DDI CNTL)

U40E LPT_PCH_M_EV REV = 5

INT_CRT_BLU T45 ← R499 150/F_4 ← (16) INT_CRT_BLU
INT_CRT_GRE U44 ← R498 150/F_4 ← (16) INT_CRT_GRE
INT_CRT_RED V45 ← R497 150/F_4 ← (16) INT_CRT_RED
INT_DDCCLK M43 ← (16) INT_DDCCLK
INT_DDCDAT M45 ← (16) INT_DDCDAT
INT_CRT_HSYNC N42 ← R500 33_4 ← PCH_HSYNC_R ← (16) INT_CRT_HSYNC
INT_CRT_VSYNC N44 ← R501 33_4 ← PCH_VSYNC_R ← (16) INT_CRT_VSYNC
DAC_IREF (50ohm)
Trace length < 500 MILS
Trace spacing = 30 MILS
DAC_IREF U40 ← R496 649/F_4
VGA_IRTN U39
CRT

LCD_PWM N36 ← (15) LCD_PWM
PANEL_BKEN K36 ← (15) PANEL_BKEN
ENVDD G36 ← (15) ENVDD
EDP_BKLTCTL
EDP_BKLTEN
EDP_VDDEN
LVDS

PIRQA# H20 ← PCI_PIRQA#
PIRQB# L20 ← PCI_PIRQB#
PIRQC# K17 ← PCI_PIRQC#
PIRQD# M20 ← PCI_PIRQD#
PCI

DGPU_HOLD_RST# A12 → R860 *0_4_S → DGPU_HOLD_RST# ← (43) DGPU_HOLD_RST#
DGPU_PWROK B13 → R861 *0_4_S → DGPU_PWROK ← (43,47) DGPU_PWROK
GFXON C12 ← GFXON ← (38,40,51) GFXON
BBS_BIT1 C10 ← (8) BBS_BIT1
DGPU_PWM_SLT# A10 → TP94
STP_A16OVR AL6 ← (8) STP_A16OVR
EC-A-14
GPIO50 (CORE)
GPIO52 (CORE)
GPIO54 (CORE)
GPIO51 (CORE)
GPIO53 (CORE)
GPIO55 (CORE)

VGA_BLUE
VGA_GREEN
VGA_RED
VGA_DDC_CLK
VGA_DDC_DATA
VGA_HSYNC
VGA_VSYNC
DISPLAY

DDPB_CTRLCLK R40 → HDMI_SCL (17)
DDPB_CTRLDATA R39 → HDMI_SDA (17)
DDPC_CTRLCLK R35
DDPC_CTRLDATA R36
DDPD_CTRLCLK N40 → TP89
DDPD_CTRLDATA N38 → TP59
DDPB_AUXN H45
DDPC_AUXN K43
DDPD_AUXN J42
DDPB_AUXP H43
DDPC_AUXP K45
DDPD_AUXP J44
DDPB_HPD K40 ← INT_HDMI_HPD (17)
DDPC_HPD K38
DDPD_HPD H39

(CORE) PIRQE#/GPIO2 G17 GPIO2
(CORE) PIRQF#/GPIO3 F17 GPIO3
(CORE) PIRQG#/GPIO4 L15 EXTTS_SNI_DRV0_PCH
(CORE) PIRQH#/GPIO5 M15 EXTTS_SNI_DRV1_PCH
PME# AD10 → PCI_PME# → TP62
PLTRST# Y11 → PCI_PLTRST#

LPT_PCH_M_EDS/BGA 5 OF 11

When GPIO[5:2] are configured as output GPIOs, they behave in an open drain manner.

PLTRST# Buffer

+3V_S5 → C692 0.1U/10V_4
PCI_PLTRST# → U42 TC7SH08FU → PLTRST# (2,20,23,25,26,43)
R632 100K_4

GPIO50 DGPU_HOLD_RST#_R

R235 100K_4 DGPU_HOLD_RST#
+3V R236 *10K_4

PCH PM PU/PD

+3V: SYS_RESET# R617 1K_4, CLKRUN# R256 8.2K_4
+3V_S5: WLAN_AOAC_ON R298 10K_4, PCH_BATLOW# R273 8.2K_4, PCIE_WAKE# R602 1K_4
EC-A-09
+3V_S5: PCH_RI# R582 10K_4, SUSACK#_R R625 10K_4, PCH_SUSPWRACK R603 10K_4, PCH_ACPRESENT R274 8.2K_4, SYS_PWROK R263 *100K_4, PCH_RSMRST# R291 10K_4, DELAY_VR_PWRGOOD R299 10K_4, R344 *100K_4

SYSPWOK

+3V_S5 → C426 *0.1U/10V_4
(34) SYS_PWROK → U18 TC7SH08FU → DELAY_VR_PWRGOOD → DELAY_VR_PWRGOOD (37)
EC_PWROK → EC_PWROK (18,27)
R336 *100K_4
R353 *0_4

PCH_PWROK_OK(CLG)

+3V_S5 → C427 0.1U/10V_4
EC_PWROK_R → U19 TC7SH08FU → HWPG (27,31,33,34,35,36)
DELAY_VR_PWRGOOD
EC-D-24
APWROK
R338 *0_4/S
EC_PWROK_R
DELAY_VR_PWRGOOD R362 *0_4
EC_PWROK R337 *0_4 EC_PWROK_R

DSW Circuit

SUSACK#_R R604 *0_4 PCH_SUSPWRACK
DPWROK_R → for DS3 R312 *0_4 → DPWROK (27)
R305 *0_4_S PCH_RSMRST#

PCI PU

EC-A-14
GFXON R880 *100K_4
+3V: PCI_PIRQA# R207 8.2K_4, PCI_PIRQB# R203 8.2K_4, PCI_PIRQC# R209 8.2K_4, PCI_PIRQD# R197 8.2K_4, EXTTS_SNI_DRV0_PCH R536 8.2K_4, EXTTS_SNI_DRV1_PCH R548 8.2K_4, GPIO2 R863 8.2K_4, GPIO3 R862 8.2K_4
EC-A-07

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Quanta Computer Inc.

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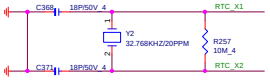
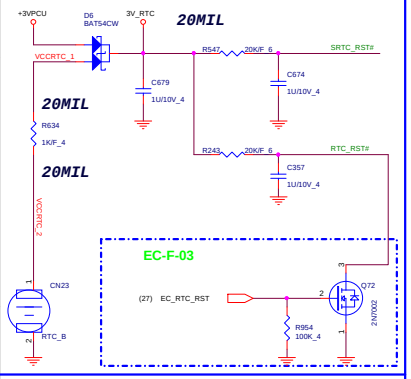
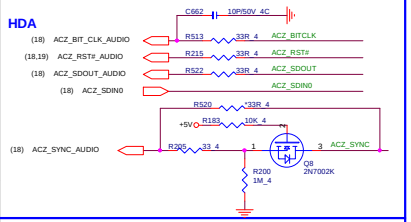
RTC Clock 32.768KHz (RTC)



RTC Circuitry (RTC)

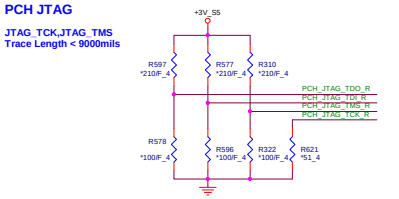


HDA

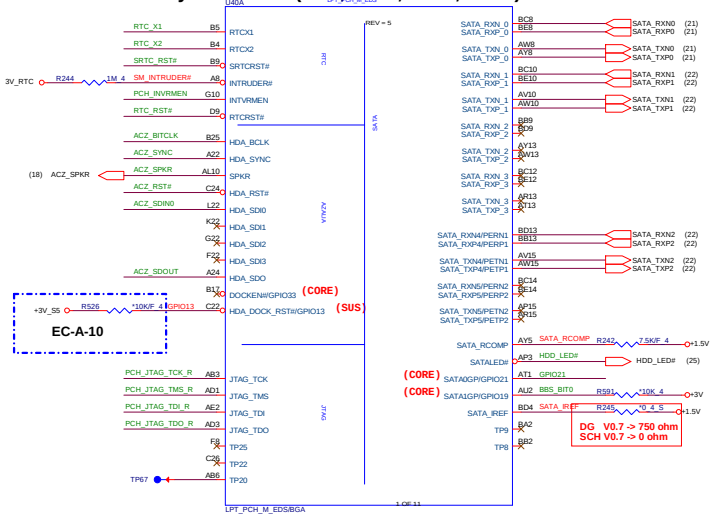


PCH JTAG

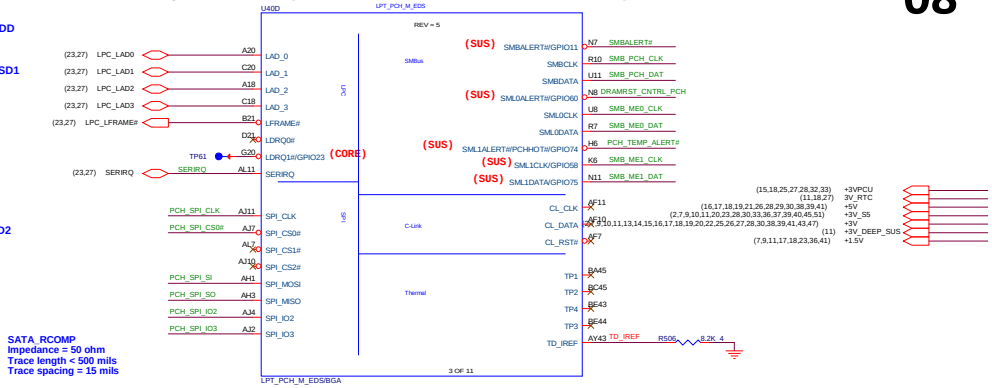
JTAG_TCK,JTAG_TMS
Trace Length < 9000mils



Lynx Point (RTC,IHDA,SATA,JTAG)



Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)

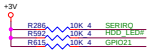


SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

PCH STRAPING

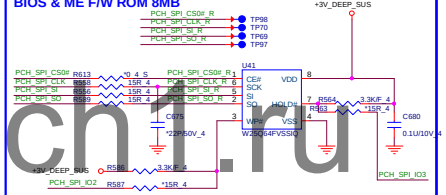
Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	ACZ_SPKR R288 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(7) SUSCLK R293 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	(7) STP_A16OVR R248 *1K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R565 *330K_4 3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 0 0 Reserved 0 1 SPI 1 0 LPC	(7) BBS_BIT1 R294 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		BBS_BIT0 R572 *1K_4
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Overrided	ACZ_SDOUT R521 *1K_4 +VCC_HDA_IO (27) ME_WR#_ (27)
GPIO36	RSVD	PWROK	Internal PD	(10) GPIO36 R573 *1K_4 +3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	(10) FDI_OVRVLTG R576 *1K_4 +3V
GPIO8	RSVD	RSMRST#	Internal PU	(10,23) BT_OFF# R321 *1K_4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(10) PLL_ODVR_EN R231 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Enable 1 = Disable Must be PU to VCCRTC	(7) DSWVREN R560 *330K_4 3V_RTC R559 *330K_4
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R201 1K_4 ACZ_SYNC

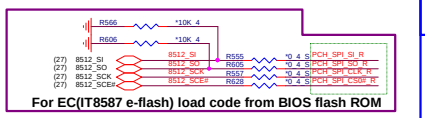
Pull High



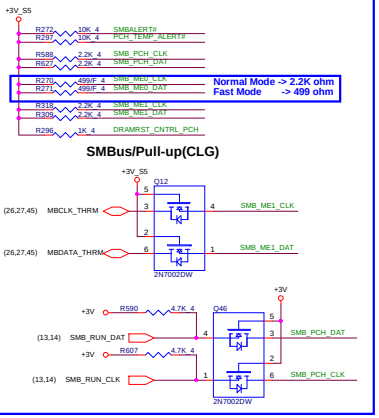
PCH Dual SPI

BIOS & ME F/W ROM 8MB





SMBus



SMBus/Pull-up(CLG)

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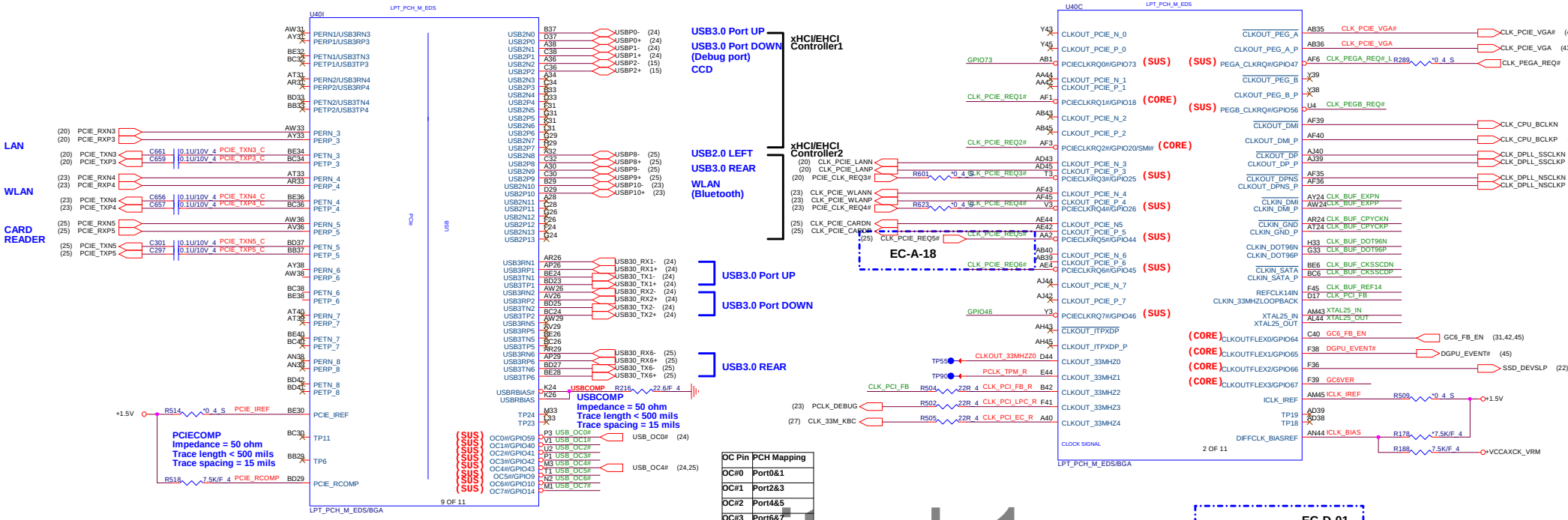
Lynx Point (PCIE,USB3.0,USB2.0)

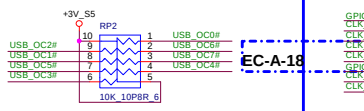
Lynx Point (CLOCK)

09

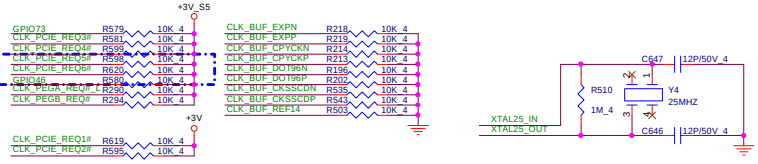


OC Pin	PCH Mapping
OC#0	Port0&1
OC#1	Port2&3
OC#2	Port4&5
OC#3	Port6&7
OC#4	Port8&9
OC#5	Port10&11
OC#6	Port12&13
OC#7	Floater OC#

USB Overcurrent



PCH Intenal Clock



PCH XDP Signal

Routed by 50 ohm

Quanta Computer Inc.	PROJECT : NL8A
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Lynx Point (GPIO,CPU/MISC,NCTF)

(2,7,8,9,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,41,43,47) +3V
(2,5,11,35,40,41) +1.05V
(2,7,8,9,11,20,23,28,30,33,36,37,39,40,45,51) +3V_S5

10

U40F — LPT_PCH_M_EDS

SGPIO R230 100_4 GPIO0	AT8	BMBUSY#/GPIO0 (CORE)	
(27) SIO_EXT_SMI#	F13	TACH1/GPIO1 (CORE)	
GPU_GX/GT	A14	TACH2/GPIO6 (CORE)	
(27) SIO_EXT_SCI#	G15	TACH3/GPIO7 (CORE)	
(8,23) BT_OFF#	Y1	GPIO8 (SUS)	
GPIO12	K13	LAN_PHY_PWR_CTRL/GPIO12 (SUS)	
(23) WLAN_ON/OFF#	AB11	GPIO15 (SUS)	
GPU_N15P/N15E	AN2	SATA4GP/GPIO16 (CORE)	
GPIO17	C14	TACH0/GPIO17 (CORE)	
BIOS_REC	BB4	SCLOCK/GPIO22 (CORE)	
(22) NGFF_SSD_PRESENT# R307 *0_4_S GPIO24	Y10	GPIO24 (SUS)	
GPIO27	R11	GPIO27 (DSW)	
(8) PLL_ODVR_EN	AD11	GPIO28 (SUS)	
(26) TEMP_ALERT#	AN6	GPIO34 (CORE)	
GPIO35	AP1	GPIO35/NMI# (CORE)	
(8) GPIO36	AT3	SATA2GP/GPIO36 (CORE)	
(8) FDI_OVRVLTG	AK1	SATA3GP/GPIO37 (CORE)	
MFG_MODE	AT7	SLOAD/GPIO38 (CORE)	
BOARD_ID1	AM3	SDATAOUT0/GPIO39 (CORE)	
BIOS_RESP	AN4	SDATAOUT1/GPIO48 (CORE)	
(15) CCD_EN	AK3	SATA5GP/GPIO49 (CORE)	
GPIO57	U12	GPIO57 (SUS)	
(15) LCD_BK_OFF	C16	TACH4/GPIO68 (CORE)	
SV_DET	D13	TACH5/GPIO69 (CORE)	
BOARD_ID2	G13	TACH6/GPIO70 (CORE)	
BOARD_ID0	H15	TACH7/GPIO71 (CORE)	

CPU/Misc — GPIO — NCTF

R549 *0_4_S TP_VSS_NCTF2

TP14	AN10	EC_A20GATE	EC_A20GATE (27)
PECI	AY1	PCH_PECI R553 *0_4	H_PECI (2,27)
RCIN#	AT6	EC_RCIN#	EC_RCIN# (27)
PROCPWRGD	AV3	TP95	H_PWRGOOD (2)
THRMTRIP#	AV1	PCH_THRMTRIP# R570 390_4	PM_THRMTRIP# (2)
PLTRST_PROC#	AU4	TP96	CPU_PLTRST# (2)
VSS	N10		

VSS: A2, A41, A43, A44, B1, B2, B44, B45, BA1, BC1, BD1, BD2, BD44, BD45, BE2, BE3, D1, E1, E45, A4

VSS: BE41, BE5, C45, A5

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LPT_PCH_M_EDS/BGA

BOARD ID SETTING

BOARD_ID0 R538 10K_4 +3V, R539 *10K_4
BOARD_ID1 R575 10K_4 +3V, R594 *10K_4
BOARD_ID2 R554 10K_4 +3V, R562 *10K_4

EC-D-01

GPIO35 R949 *10K_4

EC-E-01

BOARD_ID[3:0] Model Name

GPIO35	BOARD_ID0	BOARD_ID1	BOARD_ID2	NLx
1	0	0	0	SDV
1	0	0	1	SIV
1	0	1	0	SIT
1	0	1	1	SVT
1	1	0	0	SOVP
1	1	0	1	NL8B SDV
1	1	1	0	NL8B SIT
1	1	1	1	NL8B MV
0	0	0	0	NL9 SDV
0	0	0	1	NL9 MV
0	0	1	0	
0	0	1	1	

PCH GPIO PU/PD

+3V
SIO_EXT_SMI# R551 10K_4
SIO_EXT_SCI# R537 10K_4
TEMP_ALERT# R262 10K_4
GPIO35 R574 10K_4
LCD_BK_OFF R542 10K_4

+3V_S5
BT_OFF# R622 *10K_4
WLAN_ON/OFF# R306 10K_4
GPIO12 R561 10K_4
GPIO24 R269 10K_4
GPIO57 R308 10K_4
GPIO27 R295 10K_4

EC-B-02
CCD_EN R320 100K_4
GPIO17 R227 10K_4

PCH MISC PU/PD

+3V
EC_A20GATE R287 8.2K_4
EC_RCIN# R247 10K_4
+1.05V
PCH_THRMTRIP# R571 *1K_4

NL8 GPU N16P/N16E Select setting

GPIO16	N16P	N16E
Stuff	Ra (Hi)	Rb (Lo)

+3V — R648 Rb 10K_4 — GPU_N15P/N15E — R593 Ra *10K_4

NL8 GPU GX/GT Select setting

	GX	GT
Stuff	Ra (Hi)	Rb (Lo)

+3V — R228 Rb 10K_4 — GPU_GX/GT — R232 Ra *10K_4

BIOS RECOVERY 0 = Enable 1 = Disable
BIOS_REC R261 10K_4 +3V, R255 *0_4

Swap GPIO 0 = SGPIO 1 = Default
SGPIO R241 1K_4 +3V, R233 *0_4

MFG TEST
MFG_MODE R285 10K_4 +3V, R284 *0_4

SV Detect 0 = SV Detect 1 = Default
SV_DET R541 10K_4 +3V, R540 *0_4

BIOS_RESP 0 = BIOS RESP 1 = Default
BIOS_RESP R616 10K_4 +3V, R319 *0_4

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Quanta Computer Inc.

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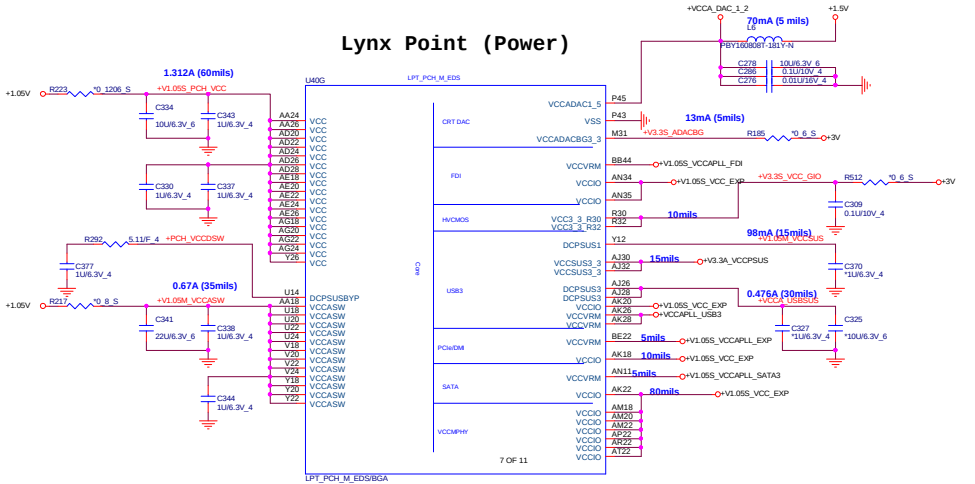
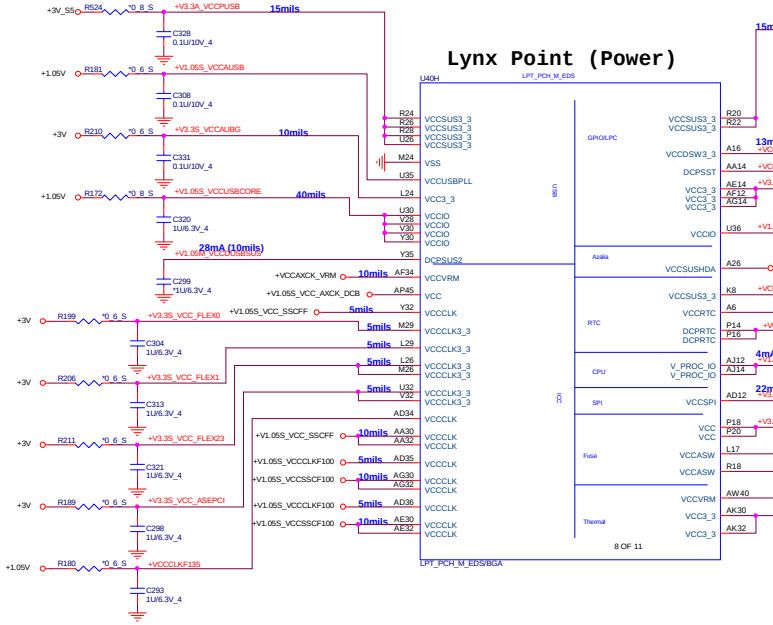
Lynx Point (Power)

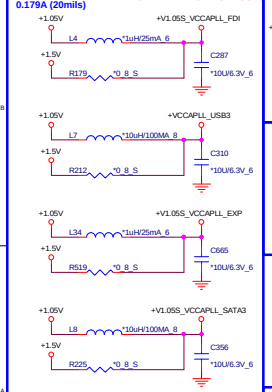




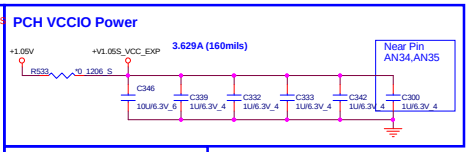
PCH VRM Power

1.05V OPTION IS PROVIDED FOR VALIDATION PURPOSES

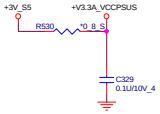
0.179A (20mils)



PCH VCCIO Power

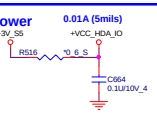


PCH band gap Power

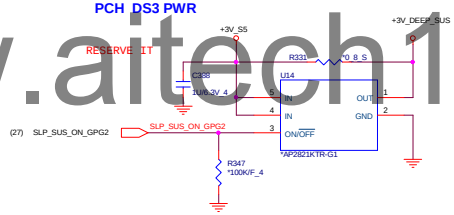


PCH HDA Power

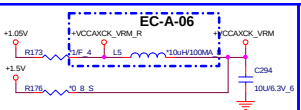
0.01A (5mils)

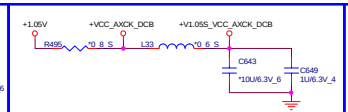


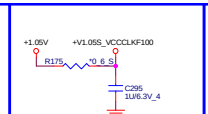
PCH_DS3 PWR

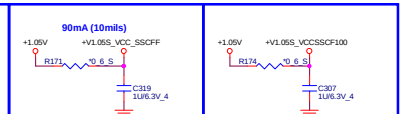


EC-A-06

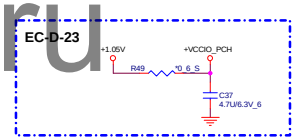


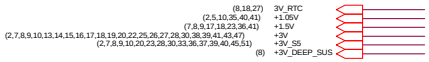






EC-D-23



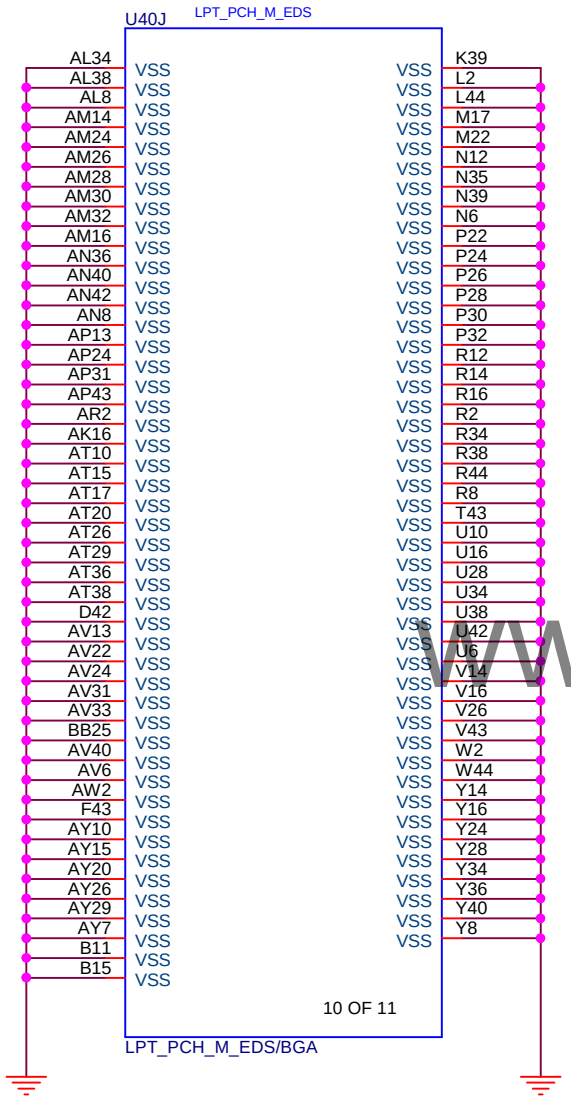


PROJECT : NL8A

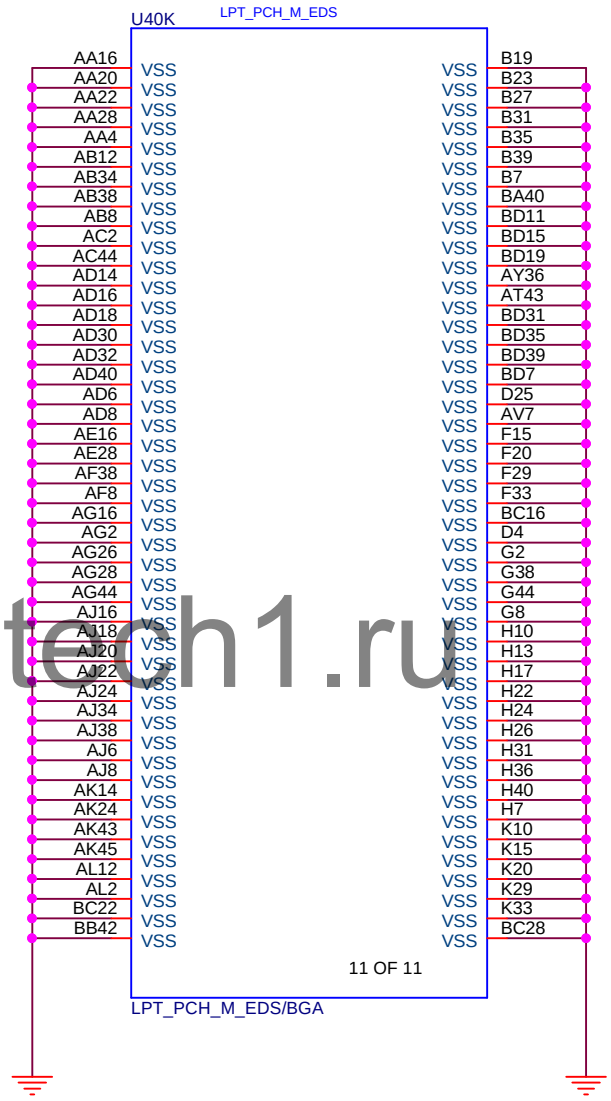
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LPT 5/6 (POWER)	3B
Date: Wednesday, January 14, 2015	Sheet 11 of 58	

Lynx Point (GND)



Lynx Point (GND)

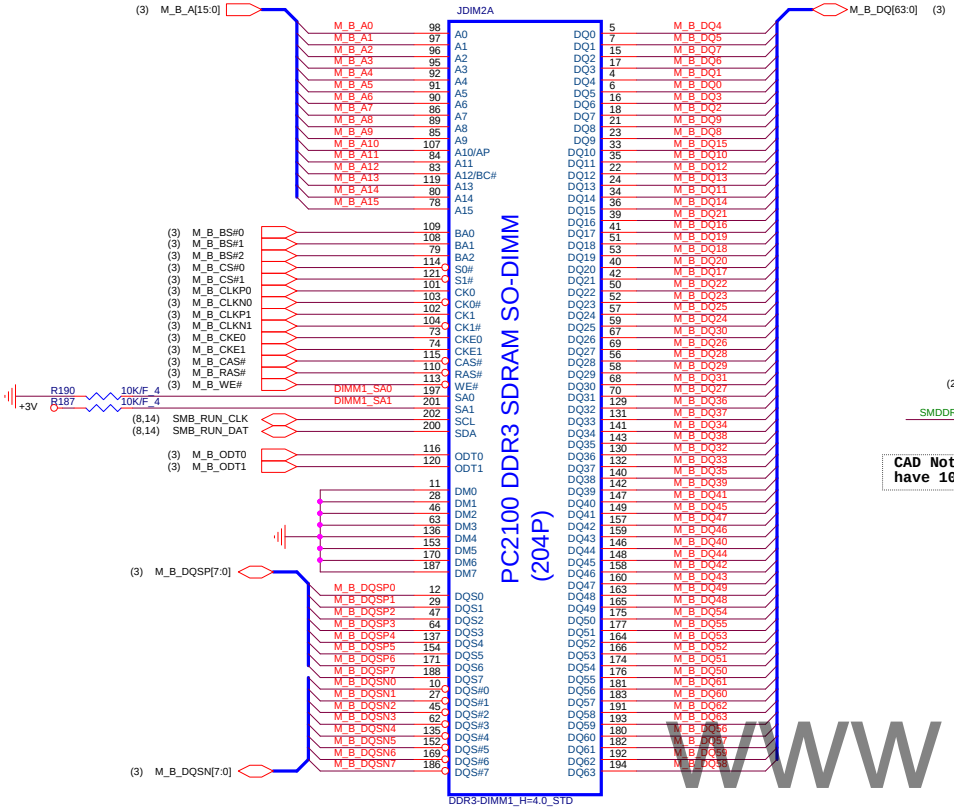


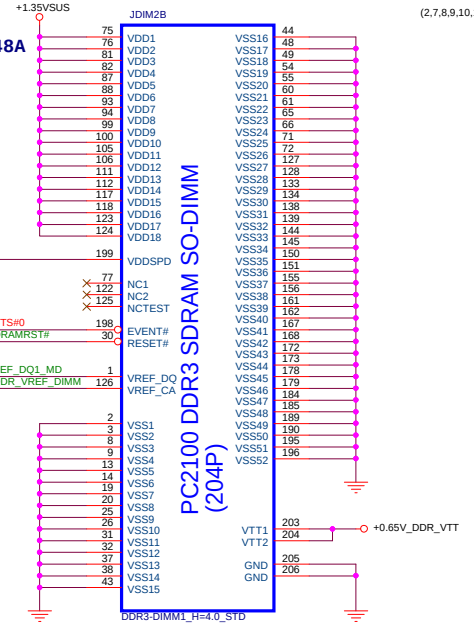
PROJECT : NL8A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LPT 6/6 (GND)	3B
Date: Wednesday, January 14, 2015	Sheet 12 of 58	

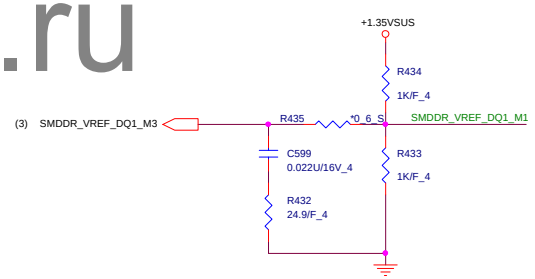
DDR_STD(DDR)



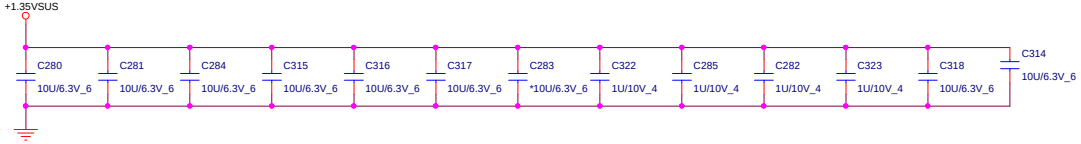


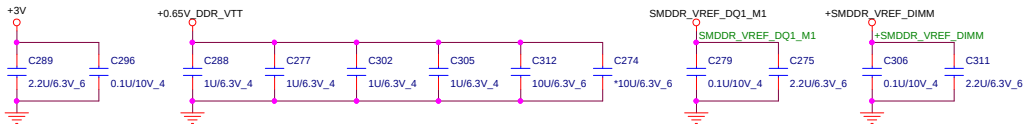
CAD Note: All VREF traces should have 10 mil trace width

(2,7,8,9,10,11,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,41,43,47) +3V
(2,5,14,34,41) +1.35VSUS
(14,34,41) +0.65V_DDR_VTT
(14,34) +SMDDR_VREF_DIMM
(8,11) +3V_DEEP_SUS



Place these Caps near SO-Dimm1

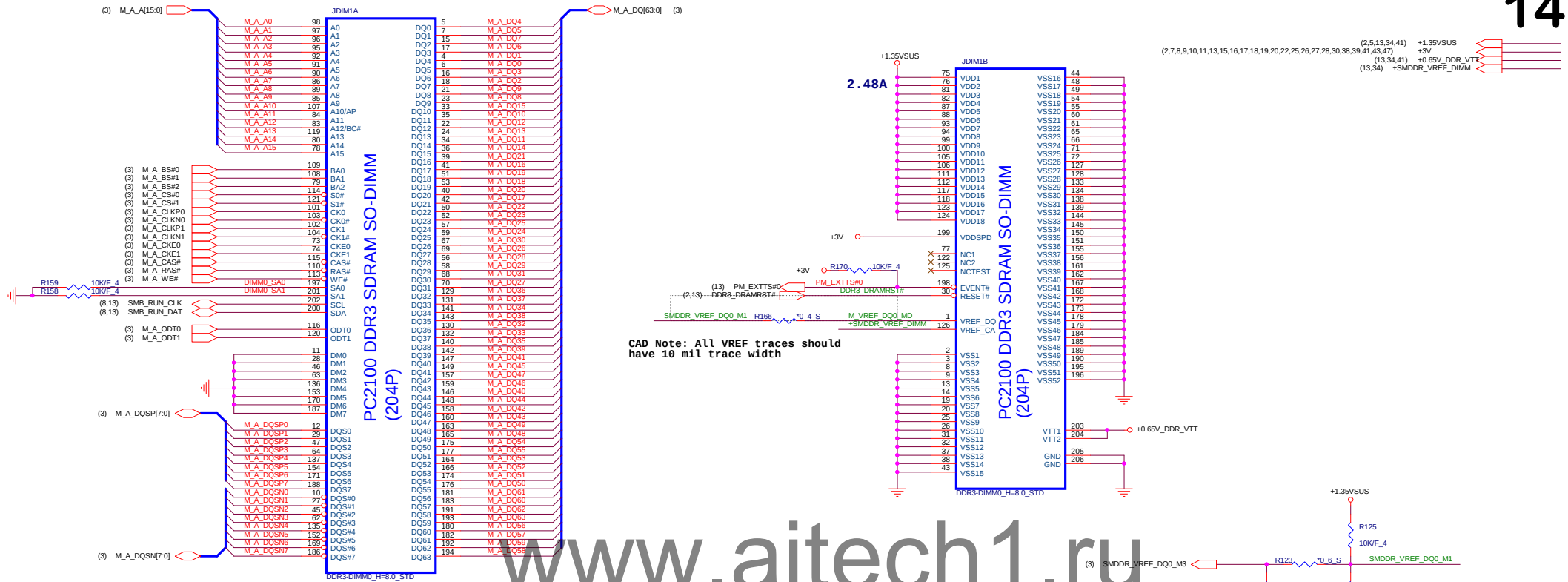




PROJECT : NL8A
Quanta Computer Inc.

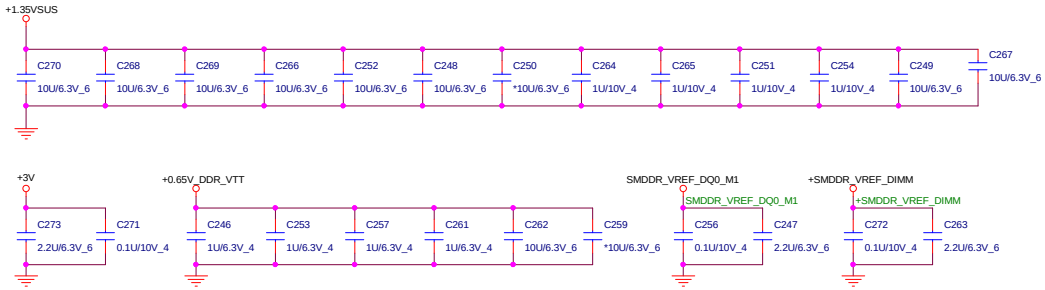
Size	Document Number	Rev
Custom	DDR3L DIMM1-STD (4.0H)	3B
Date: Wednesday, January 14, 2015	Sheet 13 of 58	

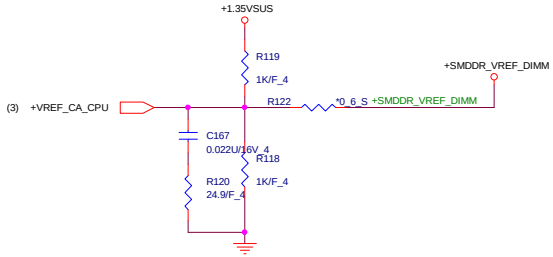
DDR_STD(DDR)



CAD Note: All VREF traces should have 10 mil trace width

Place these Caps near SO-Dimm0

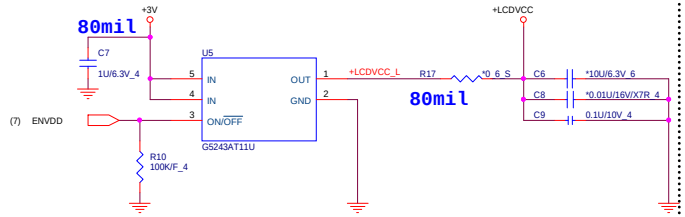




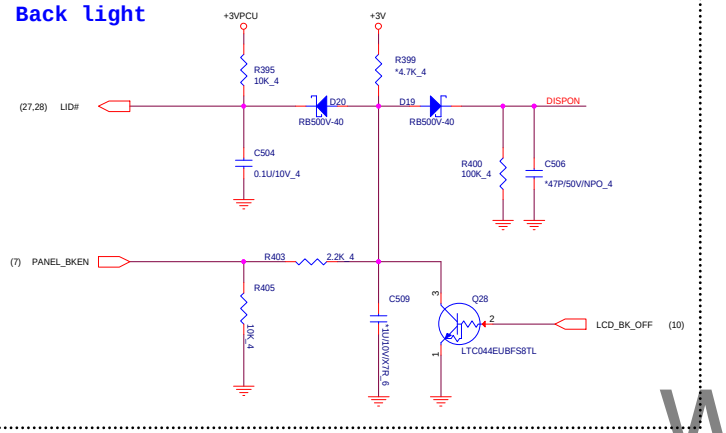
PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L DIMM0-STD (8.0H)	3B
Date: Wednesday, January 14, 2015	Sheet 14 of 58	

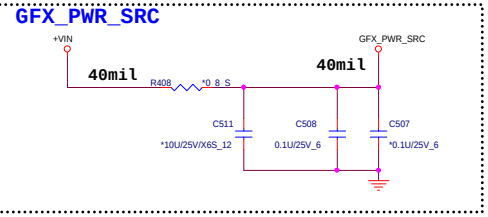
LCDVCC

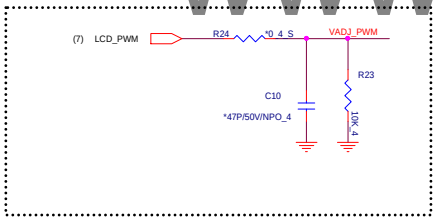


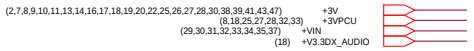
Back light

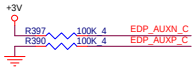


GFX_PWR_SRC

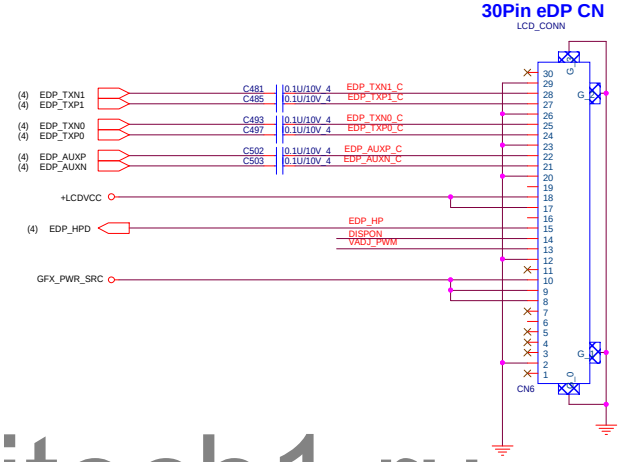




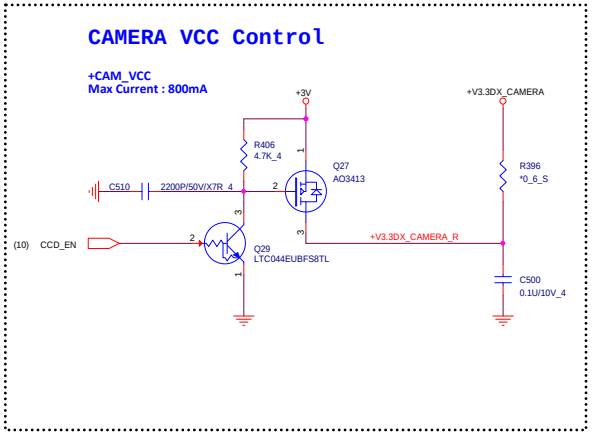




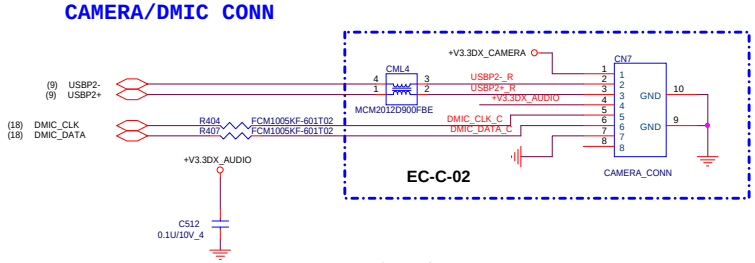
30Pin eDP CN



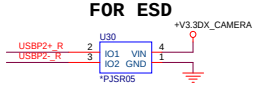
CAMERA VCC Control



CAMERA/DMIC CONN



FOR ESD



PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	eDP LCD/CAMERA	3B
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(8,17,18,19,21,26,28,29,30,38,39,41) +5V
(2,7,8,9,10,11,13,14,15,17,18,19,20,22,25,26,27,28,30,38,39,41,43,47) +3V

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

(7) INT_CRT_RED
(7) INT_CRT_GRE
(7) INT_CRT_BLU
(7) INT_CRT_VSYNC
(7) INT_CRT_HSYNC
(7) INT_DDCCLK
(7) INT_DDCDAT

+5V
CRT_VCC
D1 RB500V-40
C1 0.1U/10V_4
F2 FUSE1A8V_POLY
CRT_VCC_R
C2 0.1U/10V_4

L27 BLM15BA470SN1D_4
L28 BLM15BA470SN1D_4
L29 BLM15BA470SN1D_4
CRT_R1
CRT_G1
CRT_B1

R384 150/F_4
R385 150/F_4
R386 150/F_4
C469 5.6P/50V/COG_4
C470 5.6P/50V/COG_4
C471 5.6P/50V/COG_4
C464 5.6P/50V/COG_4
C463 5.6P/50V/COG_4
C462 5.6P/50V/COG_4

TP77
TP1

CN3
CRT CONN

U2 74AHCT1G125GW
U3 74AHCT1G125GW
C3 0.1U/10V_4

Place close to U8,U9 < 200 mil

VGAVSYNC_R
VGAHSYNC_R
R9 *0_4_S
R382 *0_4_S
CRTVSYNC1
CRTHSYNC1
C480 *10P/50V_4
C4 *10P/50V_4

Place close to CRT CONN < 200 mil

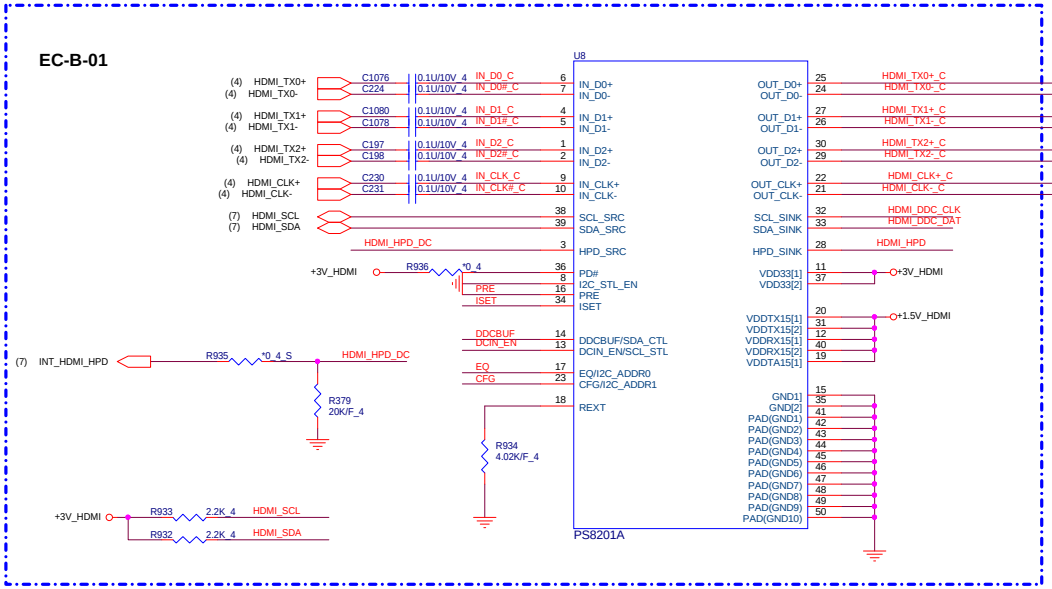
L26 HCB1608KF-121T20
L30 HCB1608KF-121T20
CRTVSYNC
CRTHSYNC
C467 10P/50V_4
C460 10P/50V_4

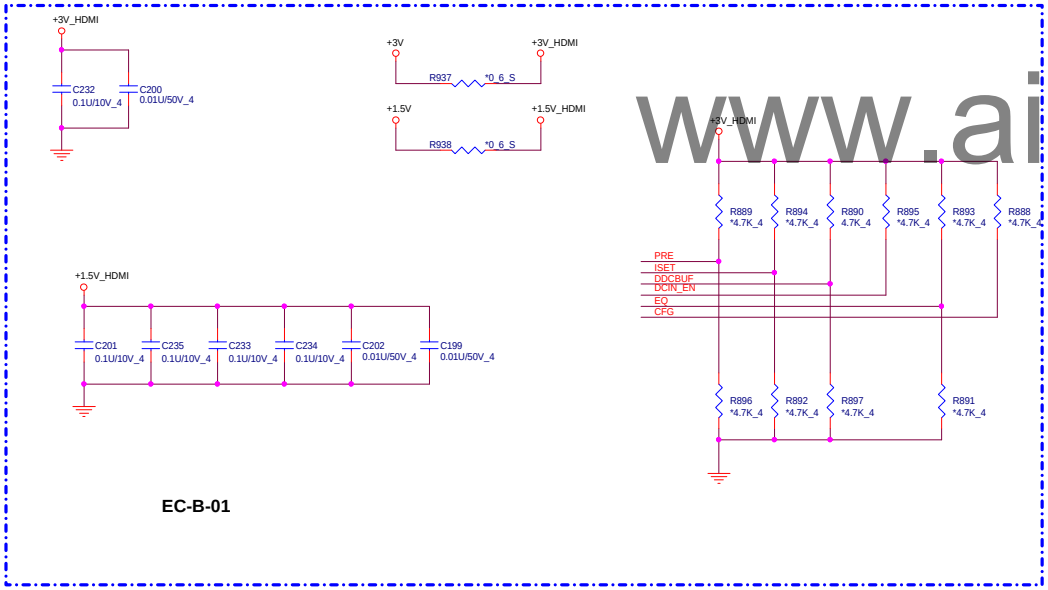
+3V
R383 2.2K_4
R389 2.2K_4
R377 4.7K_4
R378 4.7K_4
Q23A 2N7002KDW
Q23B 2N7002KDW
DDCCLK
DDCDAT
C465 *10P/50V_4
C466 *10P/50V_4

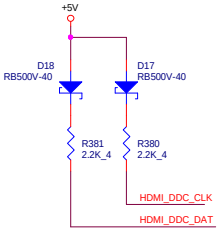
For ESD
U23
U22
*IP4220CZ6
CRT_R1
CRT_G1
CRT_B1
DDCDAT
DDCCLK
CRTVSYNC
CRTHSYNC
TP1

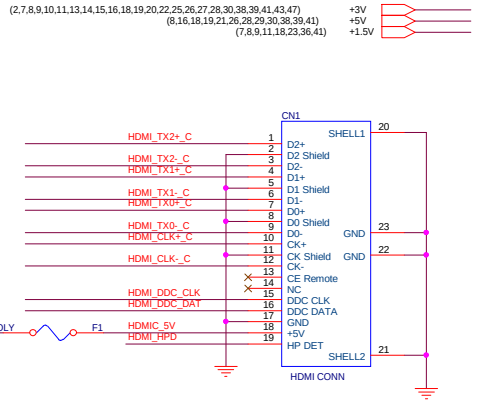
PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT CONN	3B
Date: Wednesday, January 14, 2015	Sheet 16 of 58	

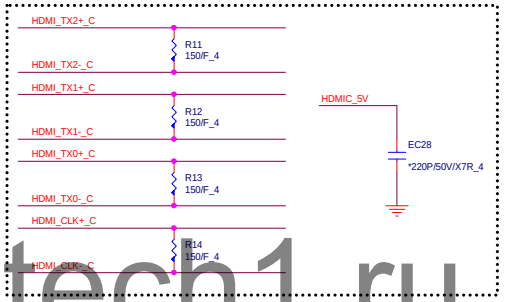


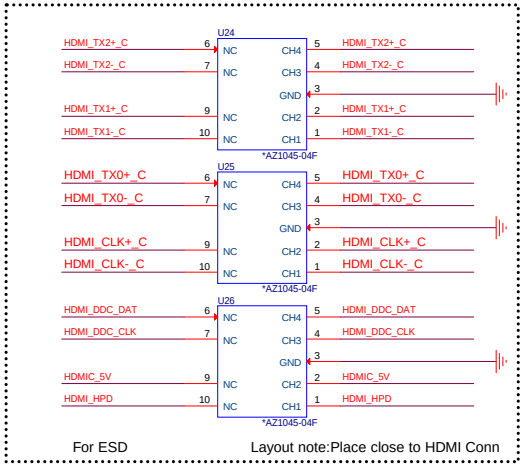






EMI reserve for HDMI





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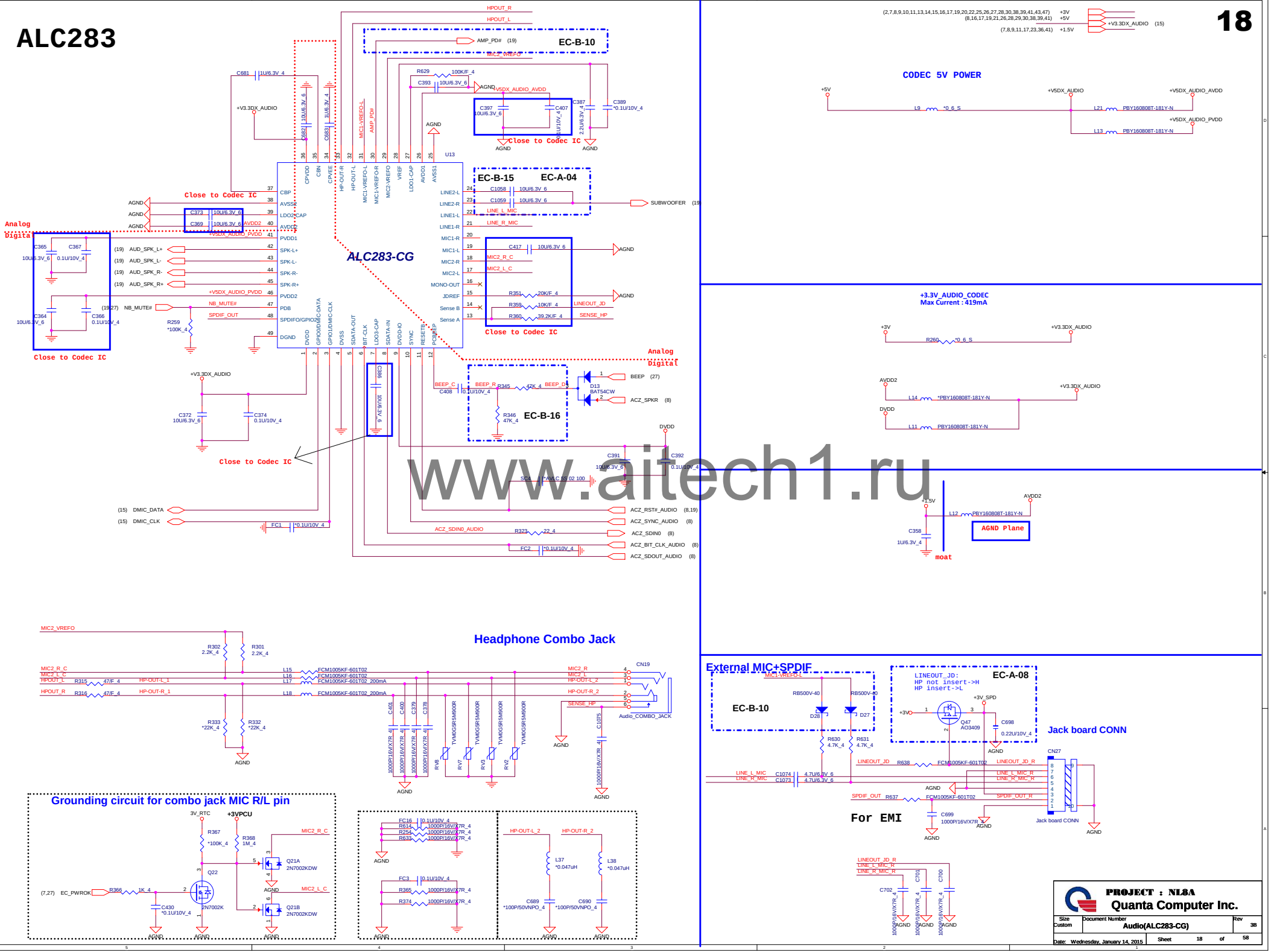
Quanta Computer Inc.		
Size: Custom	Document Number: HDMI CONN	Rev: 3B
Date: Wednesday, January 14, 2015	Sheet 17 of 58	

ALC283



Headphone Combo Jack

Grounding circuit for combo jack MIC R/L pin

External MIC+SPDIF

CODEC 5V POWER

+3.3V_AUDIO_CODEC
Max Current : 419mA

PROJECT : NL8A			
Quanta Computer Inc.			
Size: Custom	Document Number: Audio(ALC283-CG)		Rev: 3B
Date: Wednesday, January 14, 2015	Sheet 18 of 58		

Reserve for Input attenuation
To have optimization output power

Placement C4609
and then C4611

Close to IC

need to Close to connector
Reserve for EMI Depression

need to very
Close to IC

GND PAD 6 VIA (2x3)
inner 12mil, outer 20mil

EC-B-13

EC-A-05

EC-B-10

EC-B-10

EC-C-04

Digital

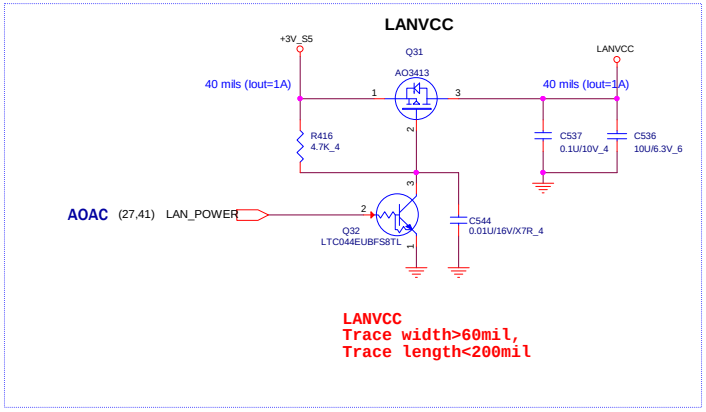
Analog

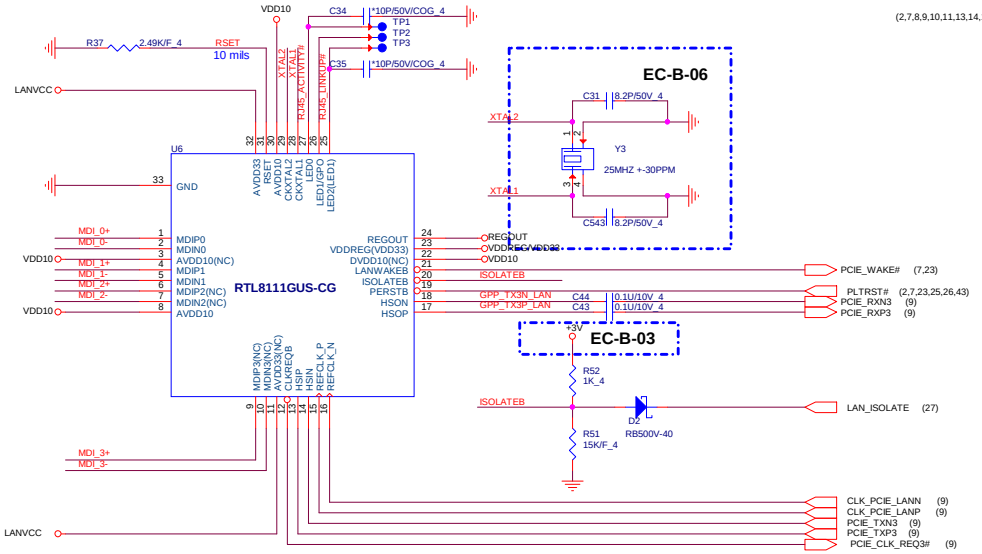
Output Gain Table

R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

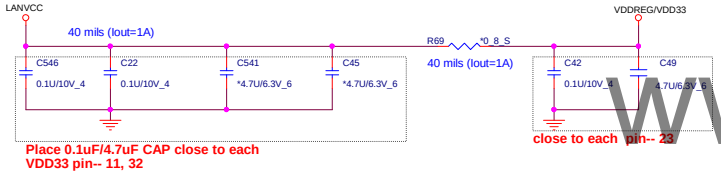
PROJECT : NL8A
Quanta Computer Inc.

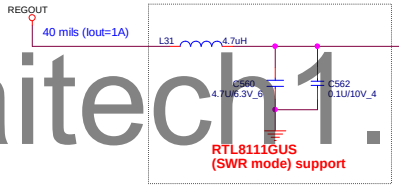
Size	Document Number	Rev
Custom	Amplifer(ALC1003)	3B
Date: Wednesday, January 14, 2015	Sheet 19 of 58	

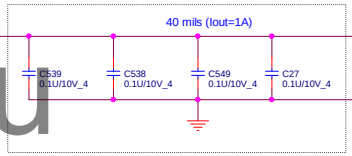


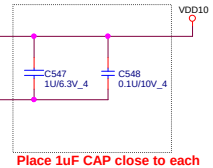


(41) LANVCC
(2,7,8,9,10,11,23,28,30,33,36,37,39,40,45,51) +3V_S5
(2,7,8,9,10,11,13,14,15,16,17,18,19,22,25,26,27,28,30,38,39,41,43,47) +3V

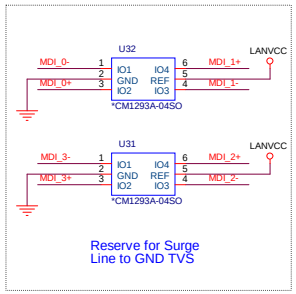


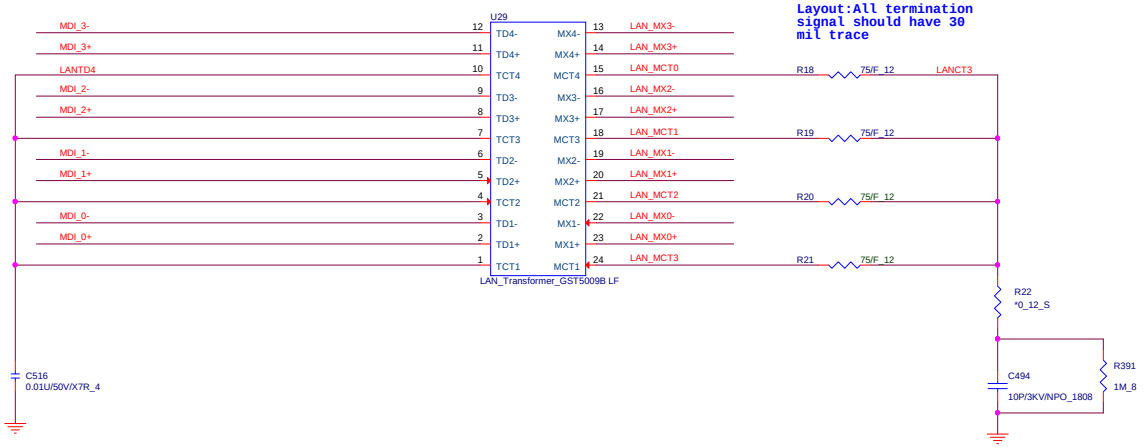




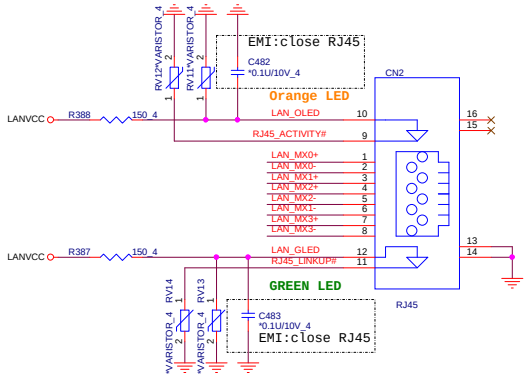


Tramsformer





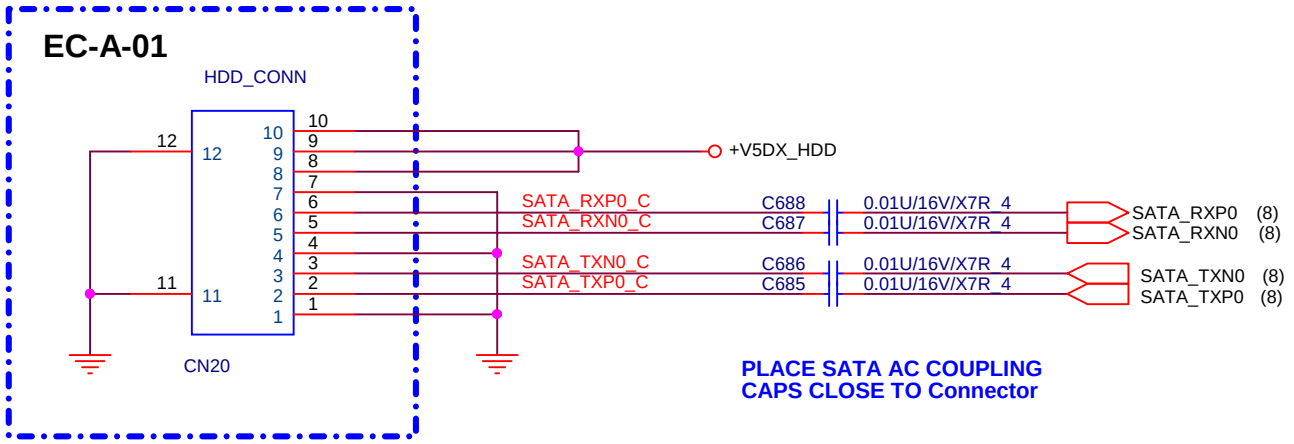
RJ45 Connector



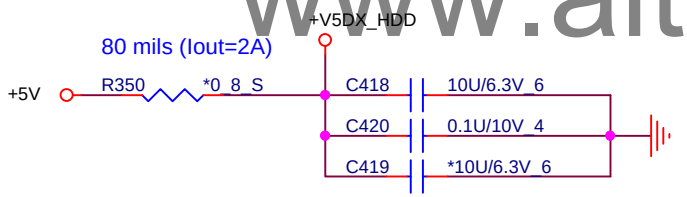
PROJECT : NL8A			
Quanta Computer Inc.			
Size: Custom	Document Number: LAN(RTL8111GUS-CG)		Rev: 3B
Date: Wednesday, January 14, 2015	Sheet: 20	of: 58	

HDD

(8,16,17,18,19,26,28,29,30,38,39,41) +5V



DC Current rating: 2 A (MAX)



PROJECT : NL8A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD	3B
Date: Wednesday, January 14, 2015	Sheet 21 of 58	

(2,7,8,9,10,11,13,14,15,16,17,18,19,20,25,26,27,28,30,38,39,41,43,47) +3V

Mini-PCIe SSD connector

120 mils (Iout=3A)

+3V

+3.3V_SSD

R398 *0_8_S

C505 1U/6.3V_4

120 mils (Iout=3A)

+3.3V_ NGFF_WWAN
Max Current : 2750mA

CN8

1	WAKE#	3.3V_1	2
3	RESERVED_1	GND0	4
5	RESERVED_2	1.5V_1	6
7	CLKREQ#	UIM_PWR	8
9	GND1	UIM_DATA	10
11	REFCLK-	UIM_CLK	12
13	REFCLK+	UIM_RESET	14
15	GND2	UIM_VPP	16
17	UIM_C8	GND3	18
19	UIM_C4	W_DISABLE#	20
21	GND4	PERST#	22
23	PERp0	3.3VAUX1	24
25	PERn0	GND5	26
27	GND6	1.5V_2	28
29	GND7	SMB_CLK	30
31	PETn0	SMB_DATA	32
33	PETp0	GND8	34
35	GND9	USB_D-	36
37	RESERVED_3	USB_D+	38
39	RESERVED_4	GND10	40
41	RESERVED_5	LED_WWAN#	42
43	RESERVED_6	LED_WLAN#	44
45	RESERVED_7	LED_WPAN#	46
47	RESERVED_8	1.5V_3	48
49	RESERVED_9	GND11	50
51	RESERVED_10	3.3V_2	52

Mini-PCIe

(8) SATA_RXP1 — 0.01U/16V/X7R_4 — C513 — SATA_RXP1_C
(8) SATA_RXN1 — 0.01U/16V/X7R_4 — C515 — SATA_RXN1_C
(8) SATA_TXN1 — 0.01U/16V/X7R_4 — C529 — SATA_TXN1_C
(8) SATA_TXP1 — 0.01U/16V/X7R_4 — C530 — SATA_TXP1_C

T3
T4

(10) NGFF_SSD_PRESENT# — R186 *0_4_S — NGFF_SSD_PRESENT#_R

+3.3V_SSD

C534 0.1U/10V_4
C514 0.047U/10V_4
C496 0.1U/10V_4
C545 0.047U/10V_4
C495 4.7U/6.3V_6

Place caps close to connector.

10K_4 R415
*0_4_S R417 SSD_DEVSLP

EC-B-11

Mini-PCIe SSD connector

120 mils (Iout=3A)

+3V

C375 1U/6.3V_4

120 mils (Iout=3A)

+3.3V_ NGFF_WWAN
Max Current : 2750mA

CN18

1	WAKE#	3.3V_1	2
3	RESERVED_1	GND0	4
5	RESERVED_2	1.5V_1	6
7	CLKREQ#	UIM_PWR	8
9	GND1	UIM_DATA	10
11	REFCLK-	UIM_CLK	12
13	REFCLK+	UIM_RESET	14
15	GND2	UIM_VPP	16
17	UIM_C8	GND3	18
19	UIM_C4	W_DISABLE#	20
21	GND4	PERST#	22
23	PERp0	3.3VAUX1	24
25	PERn0	GND5	26
27	GND6	1.5V_2	28
29	GND7	SMB_CLK	30
31	PETn0	SMB_DATA	32
33	PETp0	GND8	34
35	GND9	USB_D-	36
37	RESERVED_3	USB_D+	38
39	RESERVED_4	GND10	40
41	RESERVED_5	LED_WWAN#	42
43	RESERVED_6	LED_WLAN#	44
45	RESERVED_7	LED_WPAN#	46
47	RESERVED_8	1.5V_3	48
49	RESERVED_9	GND11	50
51	RESERVED_10	3.3V_2	52

Mini-PCIe

(8) SATA_RXP2 — 0.01U/16V/X7R_4 — C340 — SATA_RXP2_C
(8) SATA_RXN2 — 0.01U/16V/X7R_4 — C335 — SATA_RXN2_C
(8) SATA_TXN2 — 0.01U/16V/X7R_4 — C326 — SATA_TXN2_C
(8) SATA_TXP2 — 0.01U/16V/X7R_4 — C324 — SATA_TXP2_C

T6
T5

NGFF_SSD_PRESENT#_R

+3V

C663 0.1U/10V_4
C292 0.047U/10V_4
C291 0.1U/10V_4
C336 0.047U/10V_4
C290 4.7U/6.3V_6

Place caps close to connector.

*0_4_S R191 SSD_DEVSLP — SSD_DEVSLP (9)

EC-B-11

PROJECT : NL8A			
Quanta Computer Inc.			
Size: Custom	Document Number: SSD mSATA X2		Rev: 3B
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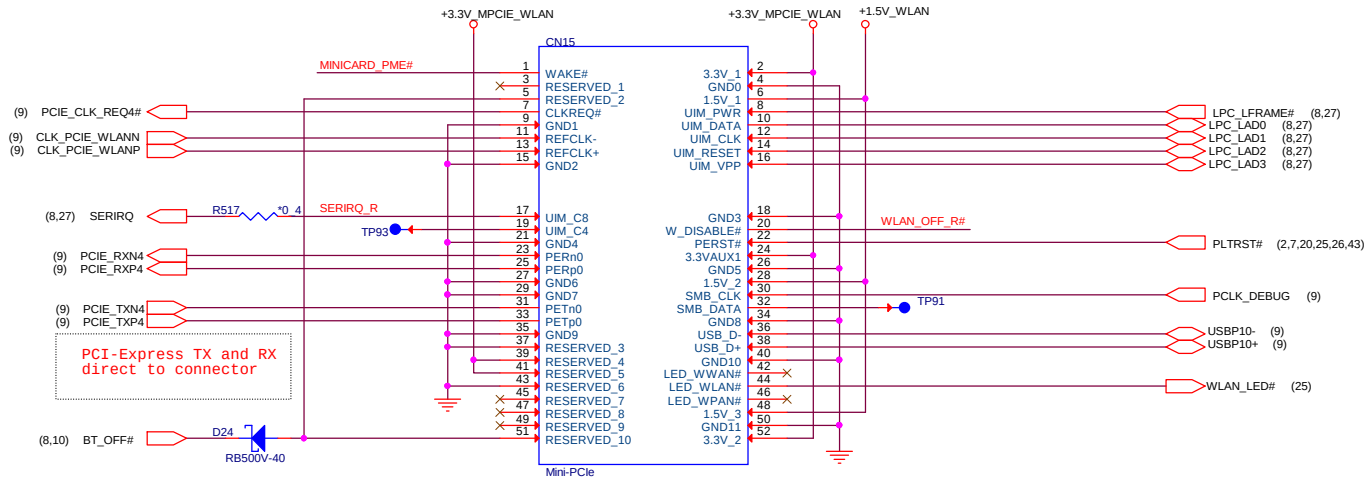
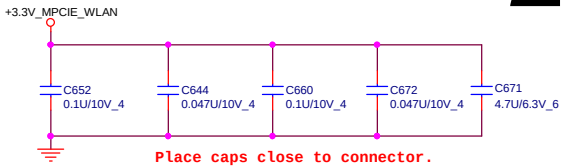
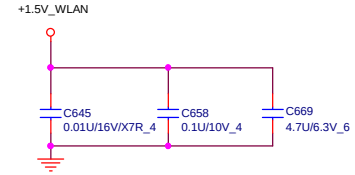
Mini PCIE Wifi/BT connector

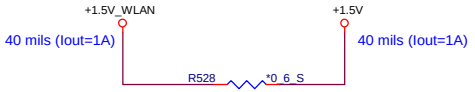


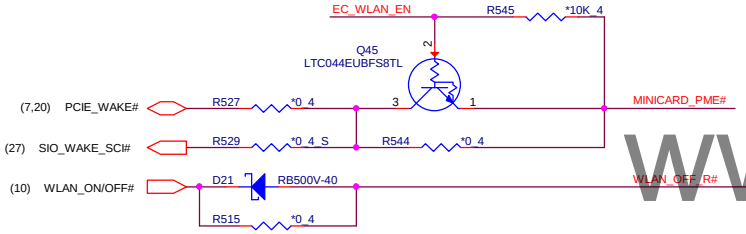
(2,7,8,9,10,11,20,28,30,33,36,37,39,40,45,51) +3V_S5
(7,8,9,11,17,18,36,41) +1.5V

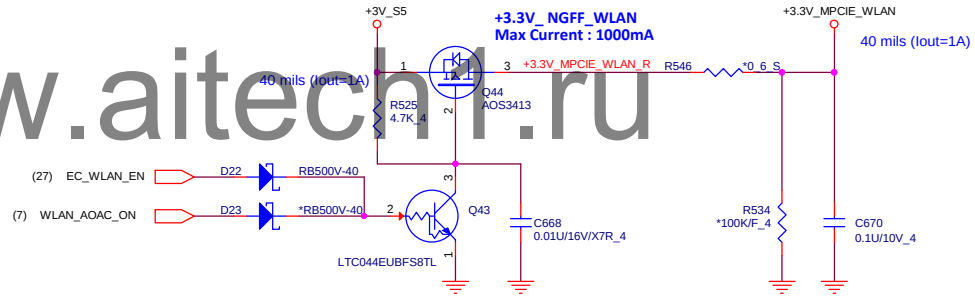
23







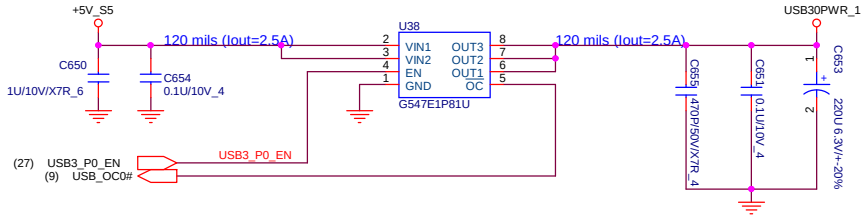


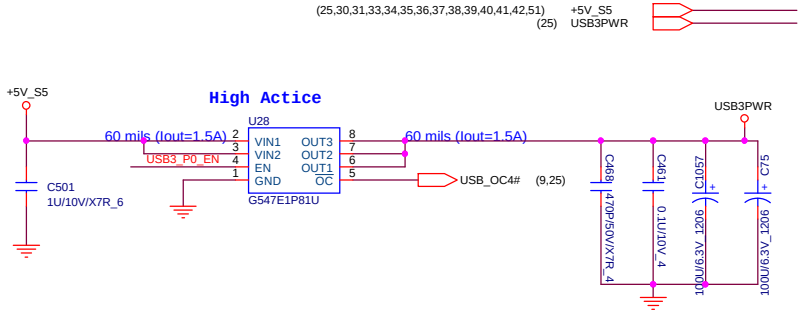


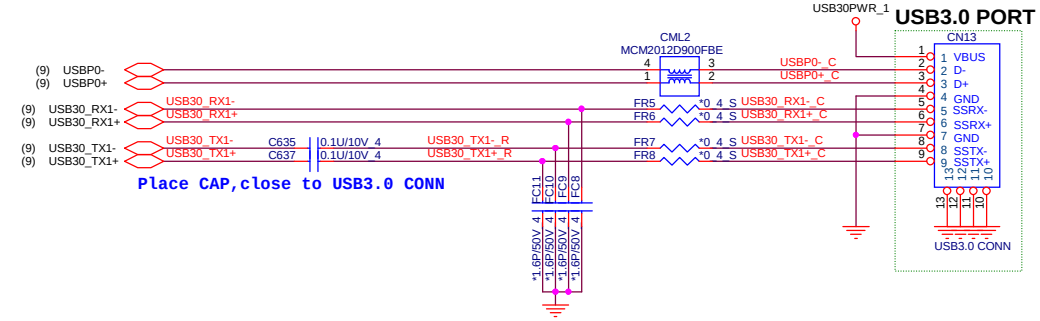
PROJECT : NL8A

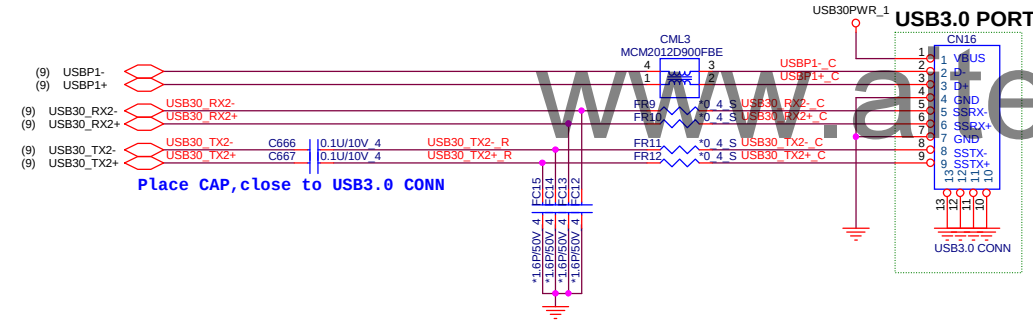
Quanta Computer Inc.

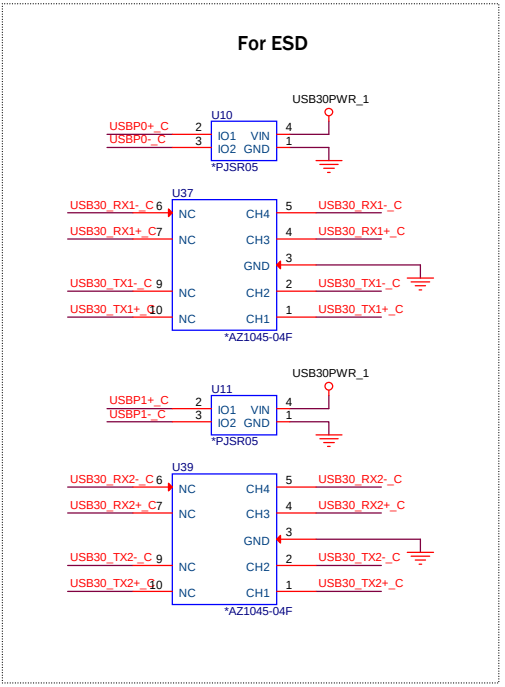
Size	Document Number	Rev
Custom	Wifi/BT MiniPCIE	3B
Date: Wednesday, January 14, 2015	Sheet 23 of 58	











EC-A-17

PROJECT : NL8A		
Quanta Computer Inc.		
Size: Custom	Document Number: USB3.0 X3	Rev: 3B
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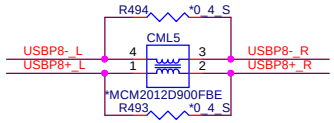
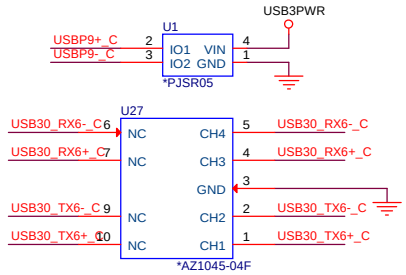
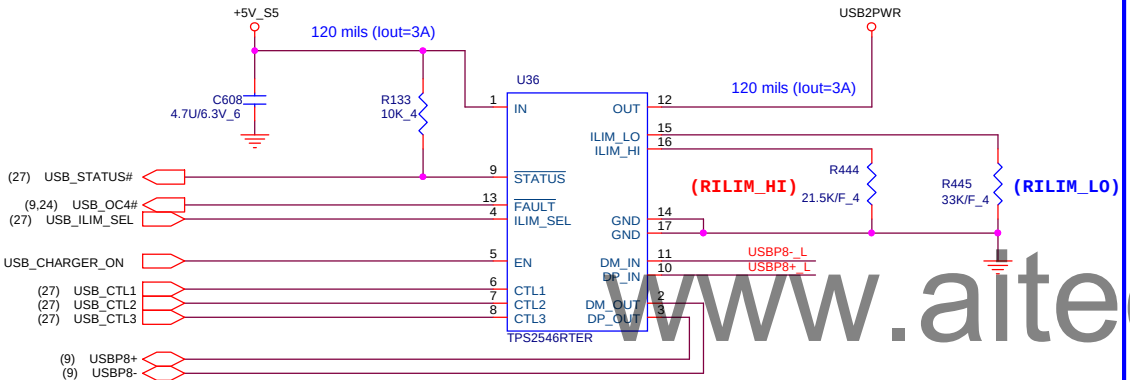




USB Charger 2.0 Port

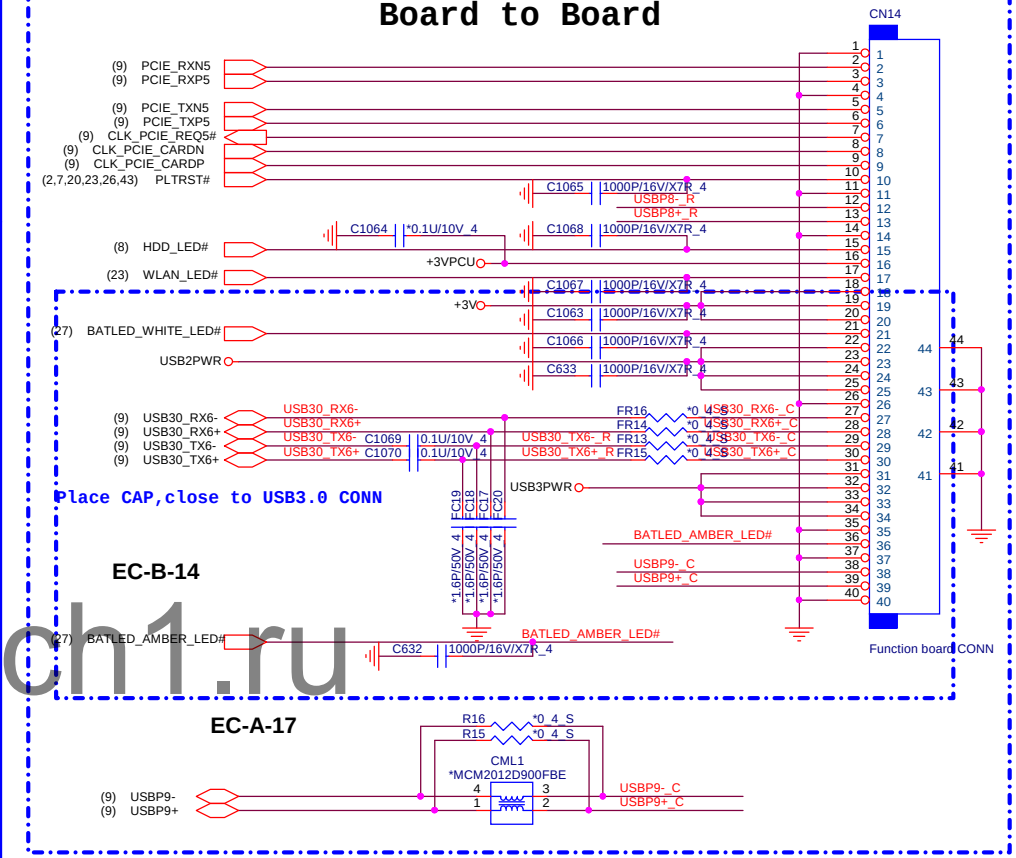


RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

(24) USB3PWR
(24,30,31,33,34,35,36,37,38,39,40,41,42,51) +5V_S5
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,26,27,28,30,38,39,41,43,47) +3V

Board to Board



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Quanta Computer Inc.		
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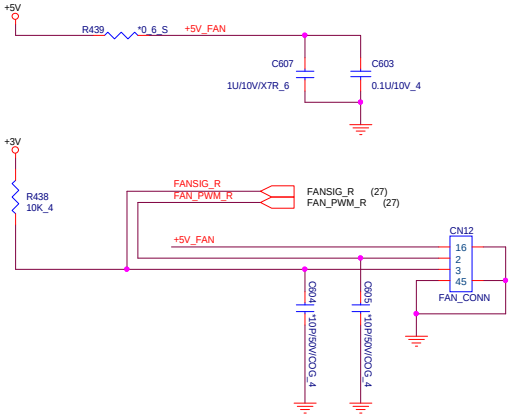
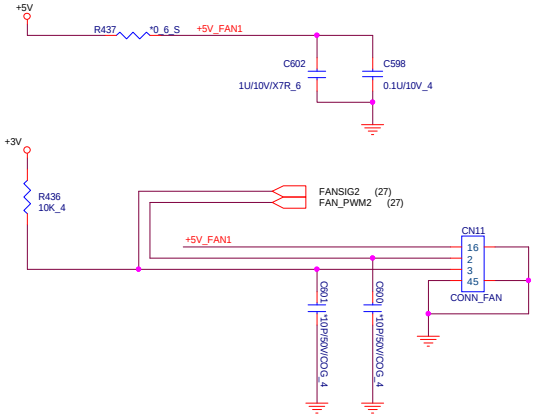
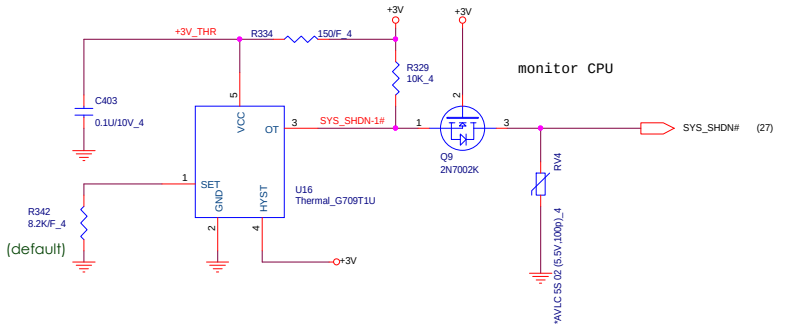
FAN CONTROL

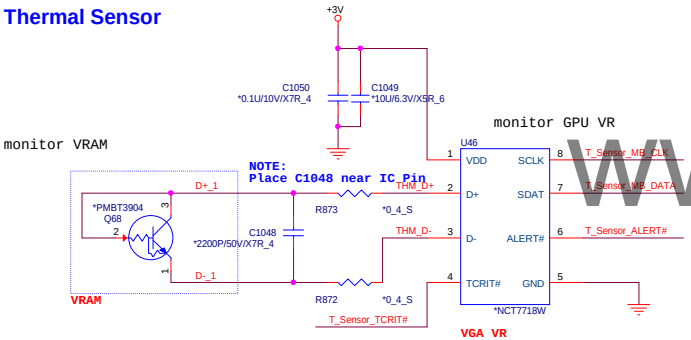




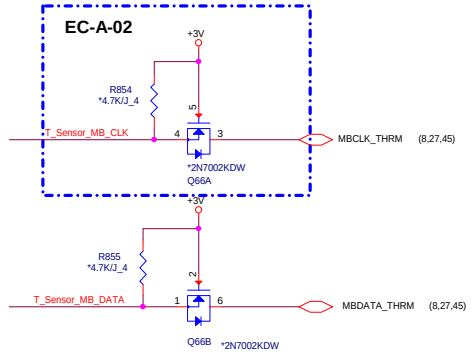
Thermal Sensor

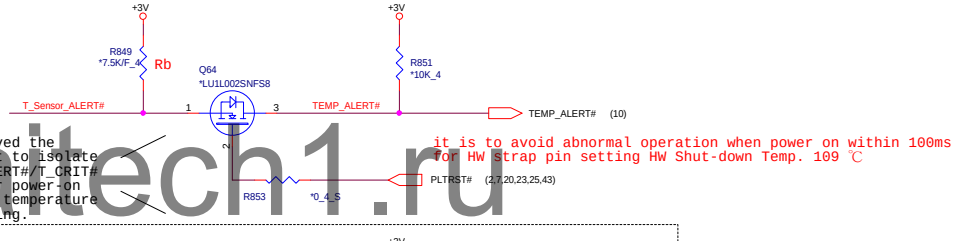


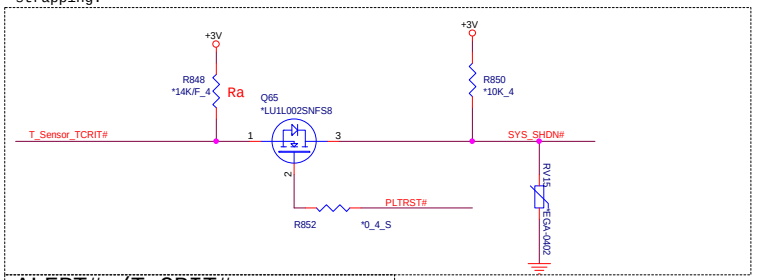
Thermal Sensor



ADDRESS: 98







*Reserved the circuit to isolate the ALERT#/T_CRIT# pin for power-on T_CRIT temperature strapping.

it is to avoid abnormal operation when power on within 100ms for HW Strap pin setting HW Shut-down Temp. 109 ℃

ALERT# /T_CRIT#
Pull-up Resistor

Rb \ Ra	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN/Thermal	3B
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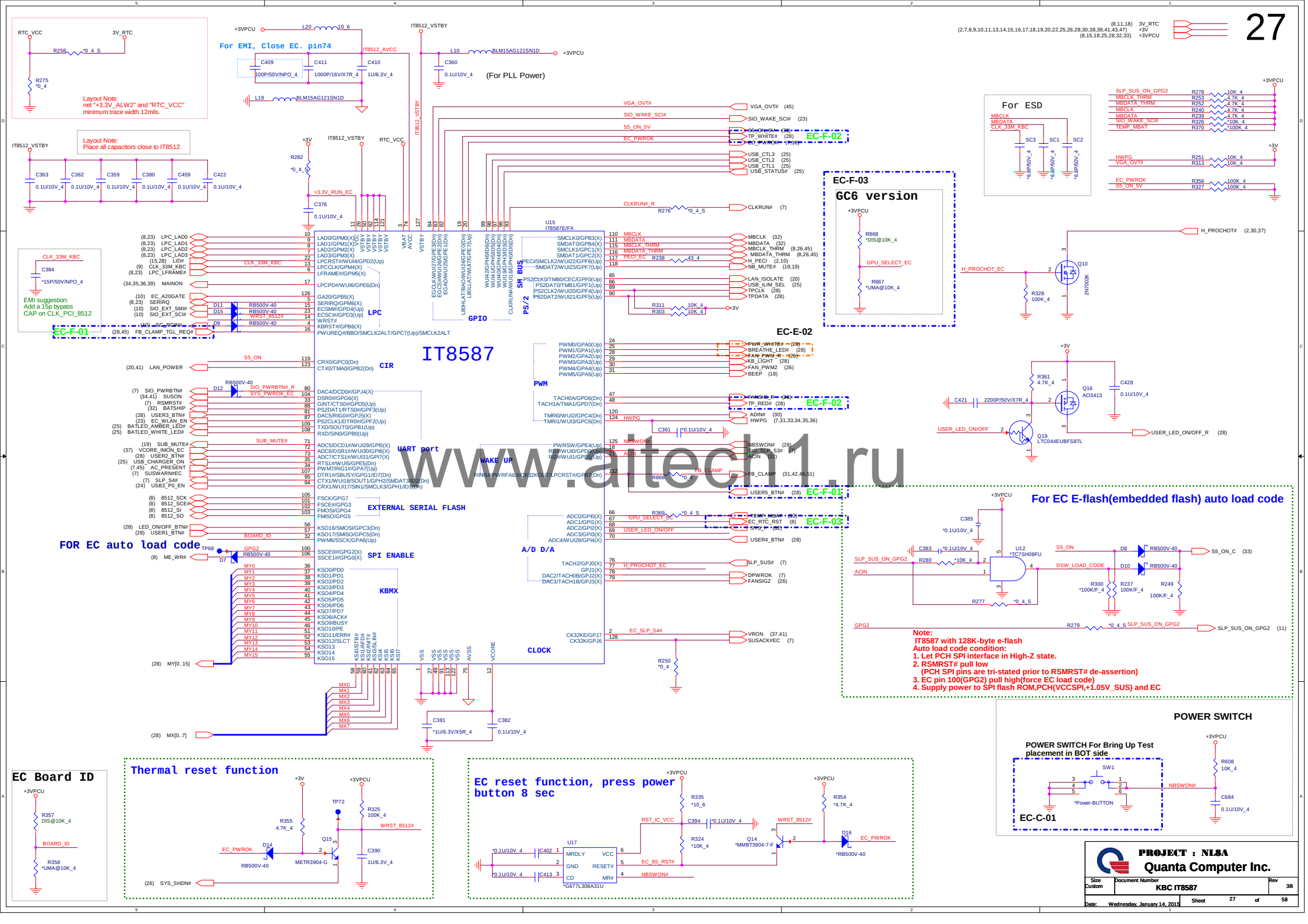

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Quanta Computer Inc.	
Size: Custom	Document Number: KBC IT8587
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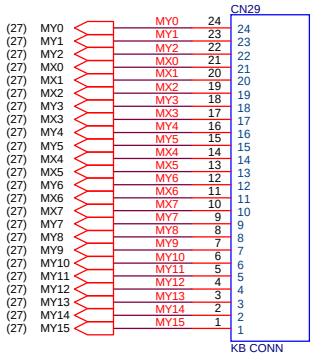
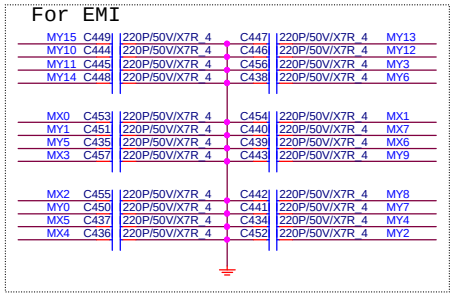
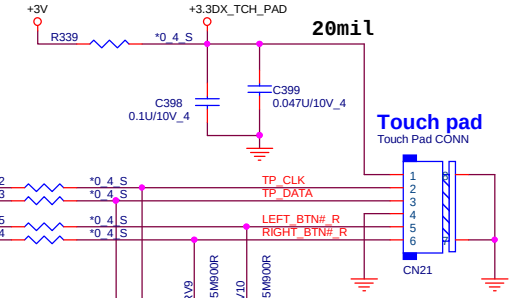
KEYBOARD



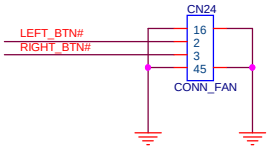


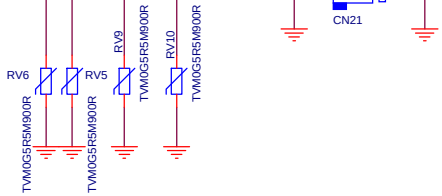
(8,16,17,18,19,21,26,29,30,38,39,41) +5V
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,30,38,39,41,43,47) +3V
(8,15,18,25,27,32,33) +3VPCU
(2,7,8,9,10,11,20,23,30,33,36,37,39,40,45,51) +3V_S5

+3V_TP
Max Current : 50mA

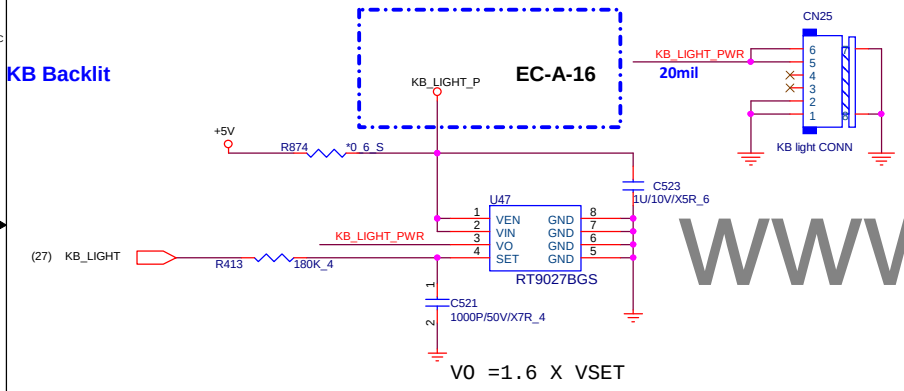


Touch button connector

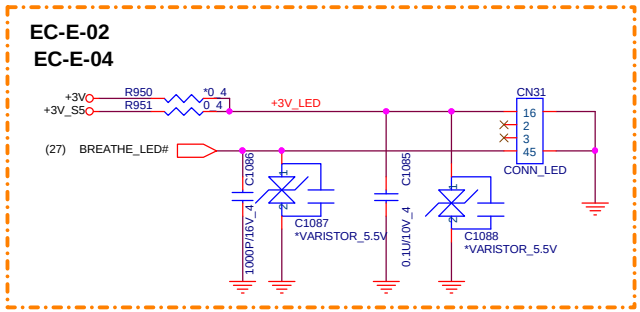




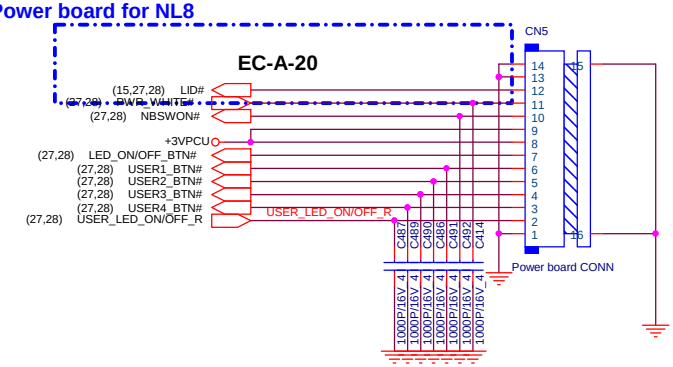
KB Backlit



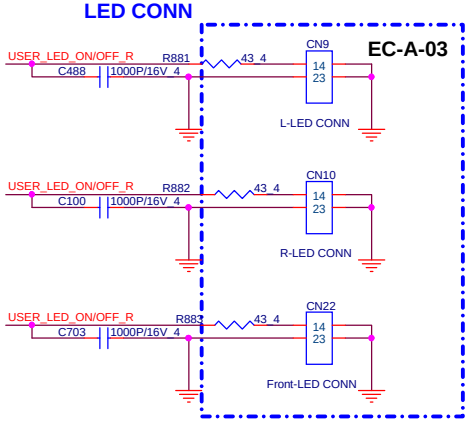
EC-F-02



Power board for NL8



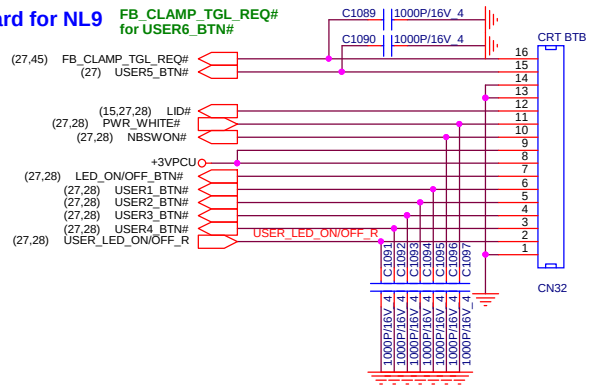
LED CONN



Power board for NL9

EC-F-01

FB_CLAMP_TGL_REQ# for USER6_BTN#



PROJECT : NL8A
Quanta Computer Inc.

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Custom	KB/TP/LID	3B
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(8,16,17,18,19,21,26,28,30,38,39,41) +5V
(15,30,31,32,33,34,35,37) +VIN

CPU BRACKET

INTEL-CPU-BKT3

H3
*INTEL-CPU-BKT3

H37
*h-c83d83n

H23
*HG-TC236BC315D110P2

H17
*HG-TC236BC315D110P2

H6
*hg-ts2bc236d110p2

H7
*spad-nl8-2np

H8
*hg-ts3bc315d110p2

H9
*spad-nl8-2np

H10
*hg-ts1bc236d110p2

H11
*spad-c315np

H20
*HG-C315D110P2

H22
*H-TC236IC150BC315D110P2

H15
*O-NL8-4

H14
*h-c83d83n

H25
*spad-nl8-1np

H24
*h-o102x83d102x83n

H16
*HG-C315D110P2

H18
H-TC197IC87BC47D47P2

H19
H-TC197IC87BC47D47P2

H21
H-TC197IC87BC47D47P2

H13
H-TC197IC87BC47D47P2

H12
*h-ts1bc83d83pt

H28
SPAD-re118x157np

H29
*SPAD-NL8-3-NP

H5
*h-tc315ic150bc150d150pt

H4
*h-tc315ic150bc150d150pt

H1
*h-tc315ic150bc150d150pt

H30
*SPAD-NL8-4-NP

H26
*spad-re196x340np

H27
*spad-re276x340np

H31
*spad-c315np

H32
*spad-c236np

H33
*spad-c236np

H35
*spad-c236np

H36
*spad-c236np

EMI

+5V

EC16	*0.1U/10V_4
EC10	*0.1U/10V_4
EC8	*0.1U/10V_4
EC6	*0.1U/10V_4
EC2	*0.1U/10V_4
EC3	*0.1U/10V_4
EC5	*0.1U/10V_4
EC1	*0.1U/10V_4
EC25	*0.1U/10V_4

+VAD

EC31	0.1U/10V_4
EC32	0.1U/10V_4
EC33	0.1U/10V_4
EC35	0.1U/10V_4
EC34	0.1U/10V_4

+VIN

EC4	0.1U/10V_4
EC7	0.1U/10V_4
EC11	0.1U/10V_4
EC26	0.1U/10V_4
EC24	0.1U/10V_4
EC27	0.1U/10V_4
EC23	0.1U/10V_4
EC17	0.1U/10V_4
EC9	0.1U/10V_4

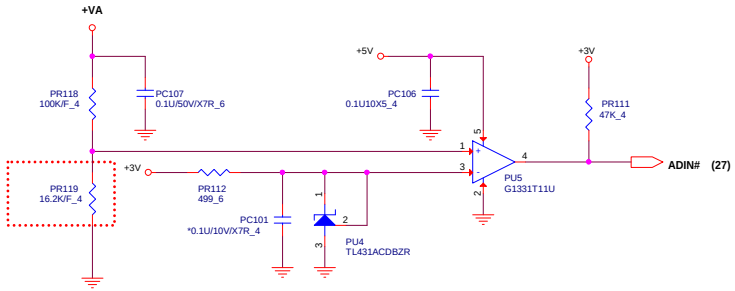
ESD

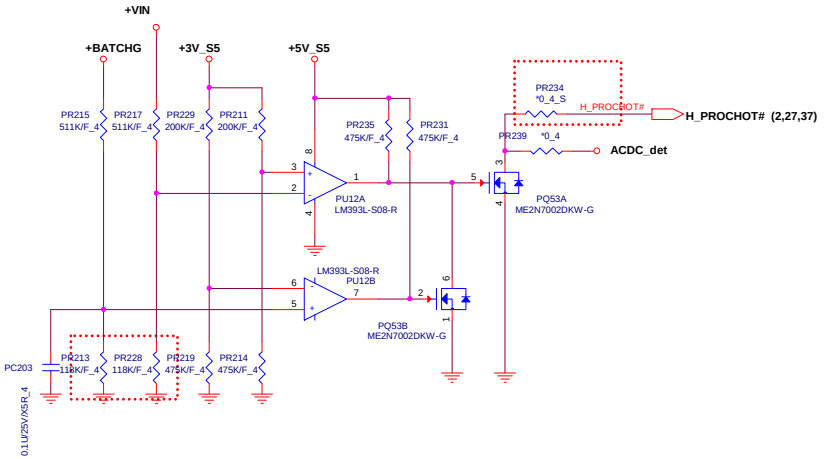
R879	*0_4_S
R876	*0_4_S
R877	*0_4_S
R878	*0_4_S

AGND

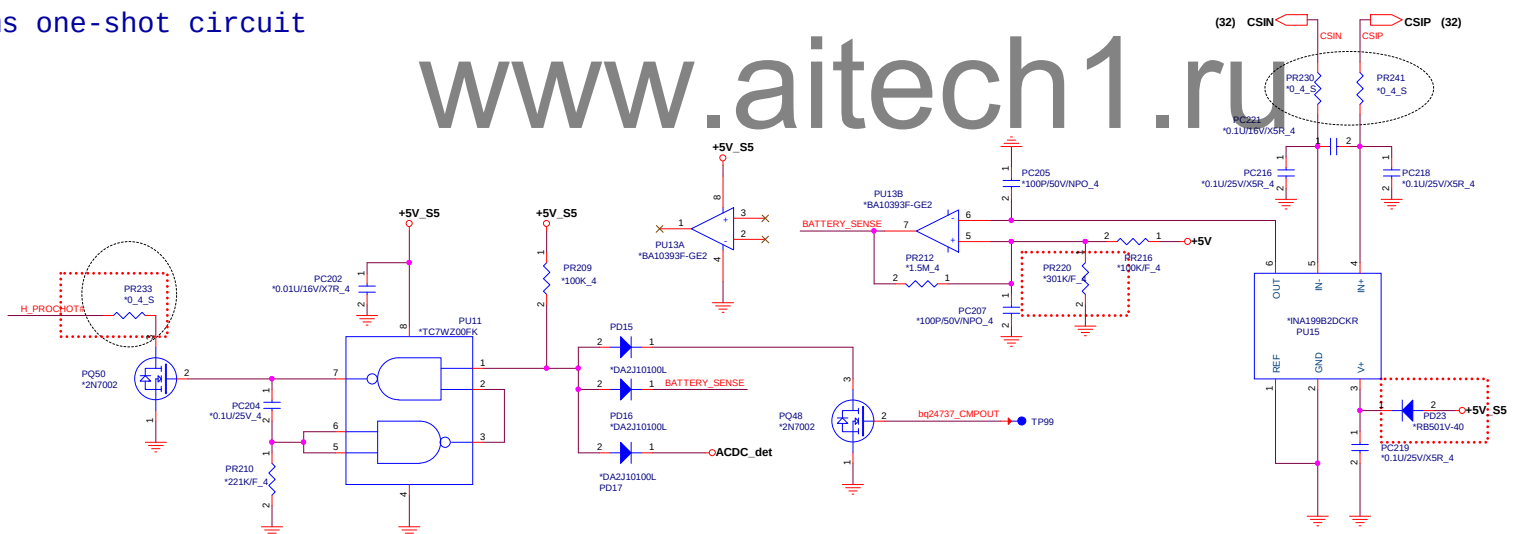
PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HOLE	3B
Date: Wednesday, January 14, 2015	Sheet 29 of 58	

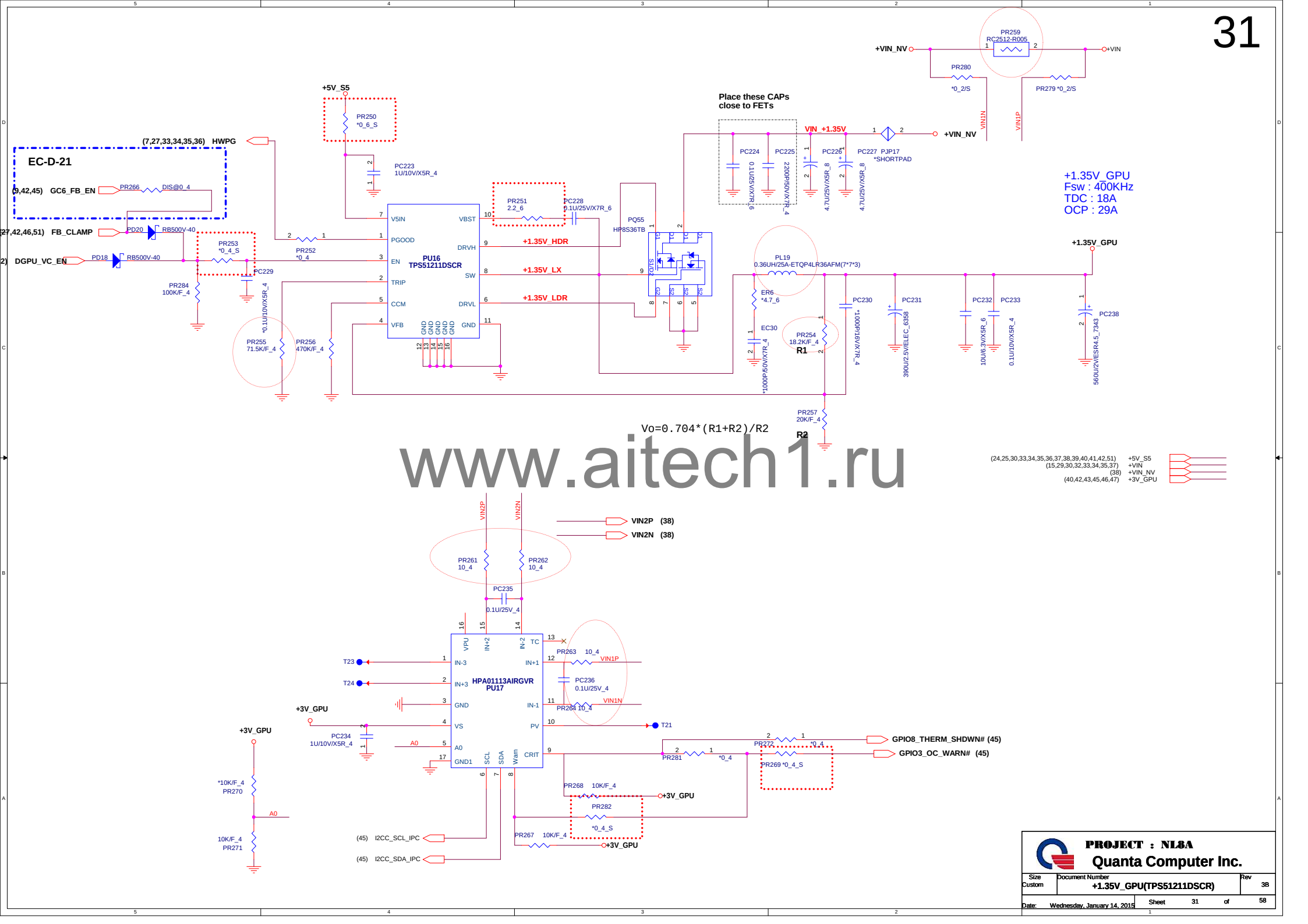




10ms one-shot circuit

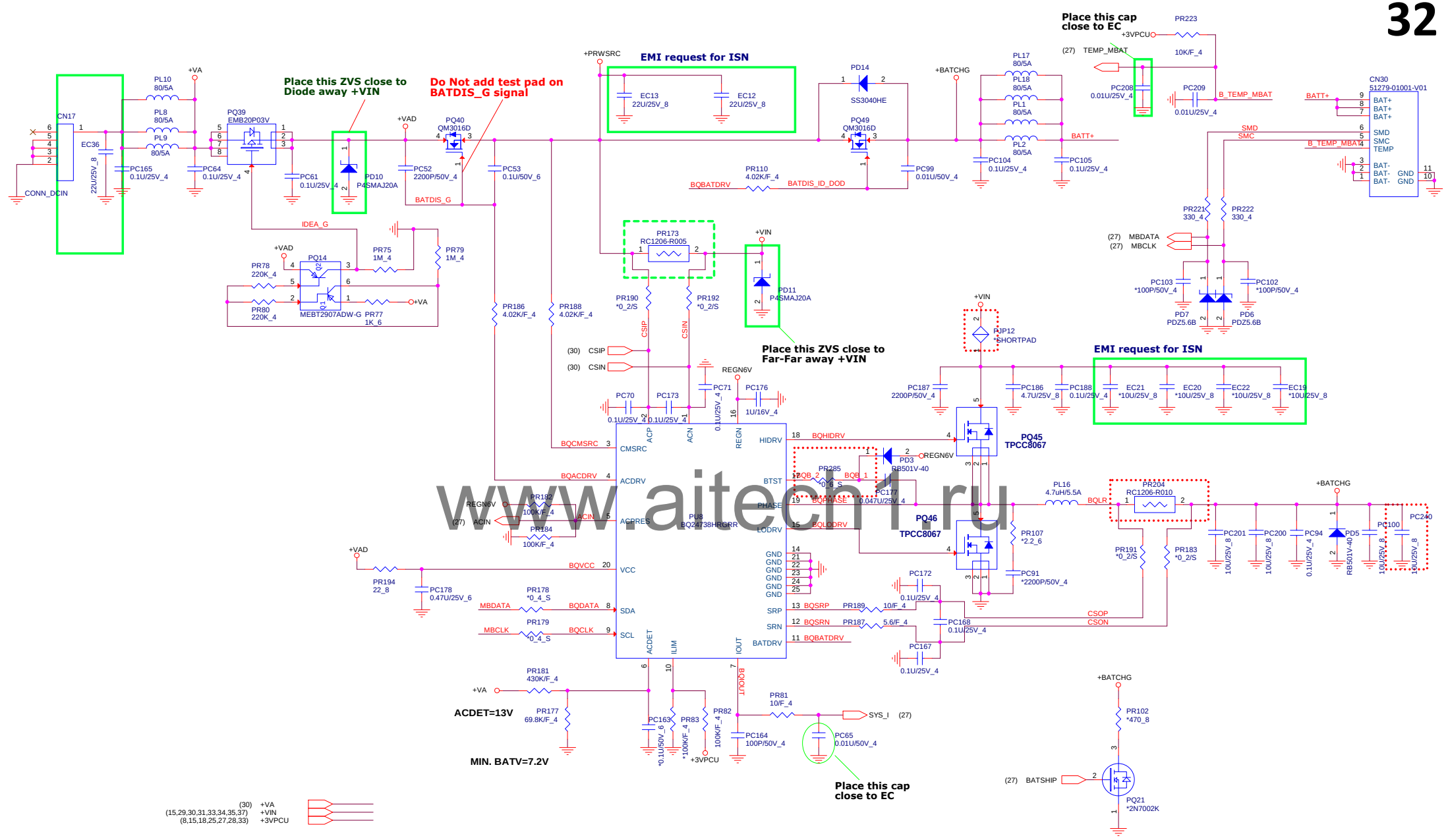


PROJECT : NL8A		
Quanta Computer Inc.		
Size: Custom	Document Number: 10ms	Rev: 3B
Date: Wednesday, January 14, 2015	Sheet 30 of 58	



PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.35V_GPU(TPS51211DSCR)	3B
Date: Wednesday, January 14, 2015	Sheet 31 of 58	



PROJECT : NL8A		
Quanta Computer Inc.		
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(15,29,30,31,32,34,35,37) +VIN
(24,25,30,31,34,35,36,37,38,39,40,41,42,51) +5V_S5
(39,40) +15V_ALW
(8,15,18,25,27,28,32) +3VPCU
(2,7,8,9,10,11,20,23,28,30,36,37,39,40,45,51) +3V_S5

5 Volt
Fsw : 400KHz
Peak : 11.3A
OCP : 15A

3.3 Volt
Fsw : 475KHz
Peak : 5.2A
OCP: 8A

Place these CAPs close to FETs

Place these CAPs close to FETs

+VIN
+3VPCU
+5VPCU
+5V_S5
+3V_S5
+15V_ALW
PJP2 *SHORTPAD
PJP1 *SHORTPAD
PJP14 *SHORTPAD
PJP10 *SHORTPAD
PC100 4.7U/25V/X5R_8
PC89 4.7U/25V/X5R_8
PC92 *0.1U/25V/X5R_4
PC191 2200p/50V/X7R_4
PC87 *0.1U/25V/X5R_4
PC189 2200p/50V/X7R_4
PC69 4.7U/25V/X5R_8
PC170 4.7U/25V/X5R_8
PR200 10_8
PR99 *0_4_S
PC82
PC80 0.1U/25V/X7R_6
PC83 4.7U/6.3V/X5R_6
4.7U/10V/X5R_6
PR108 *0_4_S
PR93 *0_4_S
S5_ON_5V (27)
S5_ON_C (27)
S5_ON_R
PQ23 TPCC8067
PQ17 TPCC8067
PQ22 TPCC8065
PQ19 TPCC8065
PC93 0.1U/25V/X7R_6
PR109 2.2/F_6
PR89 2.2/F_6
PC76 0.1U/25V/X7R_6
PU3 TPS5128SBRUKR
EN1 EN2 VIN VREG5 VREG3
DRVH1 DRVH2 VBST1 VBST2 SW1 SW2 DRVL1 DRVL2 VO1 VFB1 VFB2 PDDG VCLK CS1 CS2 GPAD
5V_DH 5V_BST 5V_LX 5V_DL TPS51275_VO1 TPS51275_VFB1
3.3V_DH 3.3V_BST 3.3V_LX 3.3V_DL TPS51275_VFB2
PL15 ETQP3W1R5WFN-1.5
PL13 NIMS0603N-2R2M
3VS5_P
PC88 0.1U/10V/X5R_4
PC86 *4.7U/10V/X5R_6
PC239 150U/6.3V/ESR38/2828
PC189 330U/6.3V_6X5.8
ER2 4.7_6
EC18 1000P/50V/X7R_4
ER5 4.7_6
EC29 1000P/50V/X7R_4
PC174 330U/6.3V_6X5.8
PC74 4.7U/6.3V/X5R_6
PC75 0.1U/10V/X5R_4
PR101 30K/F_4
PR105 19.6K/F_4
PR106 22.1K/F_4
PR90 13K/F_4
PR87 *100K/F_4
PR92 *0_4_S
PR97 13K/F_4
PR95 20K/F_4
RV1 *AVC-SS-07 (5.9V-109)_4
HWPG (7,27,31,34,35,36)
PC195 0.1U/25V/X5R_4
PR207 *0_6_S
VCLK
PD4 BAT54SW-L
PD13 BAT54SW-L
PC192 0.1U/25V/X5R_4
PC98 0.1U/25V/X5R_4
PR208 22_8
+15V_ALWP
PC97 0.1U/25V/X5R_4
PR196 *39K/F_4
S5_ON_R

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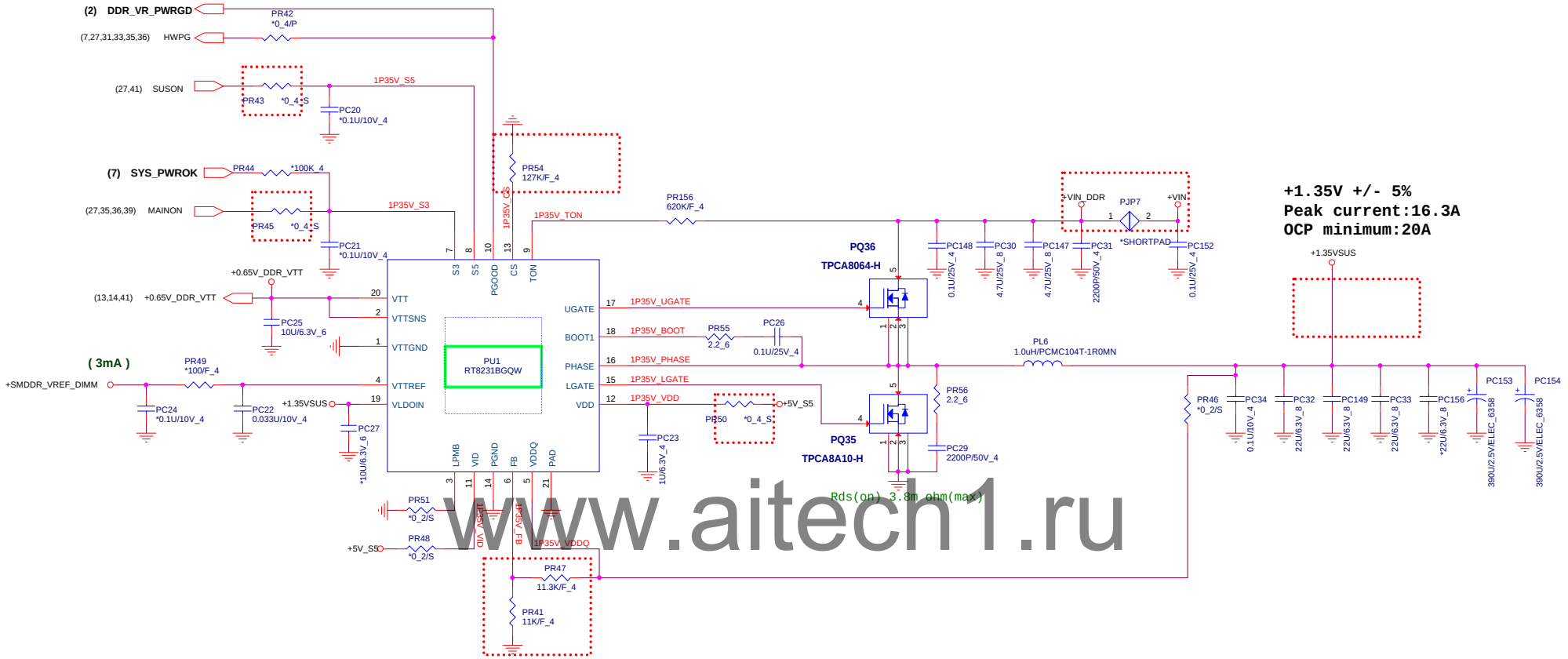
(2,5,13,14,41) +1.35VSUS
(24,25,30,31,33,35,36,37,38,39,40,41,42,51) +5V_S5
(15,29,30,31,32,33,35,37) +VIN



PROJECT : NL8A		
Quanta Computer Inc.		
Size: Custom	Document Number: DDR3 (RT8231B)	Rev: 3B
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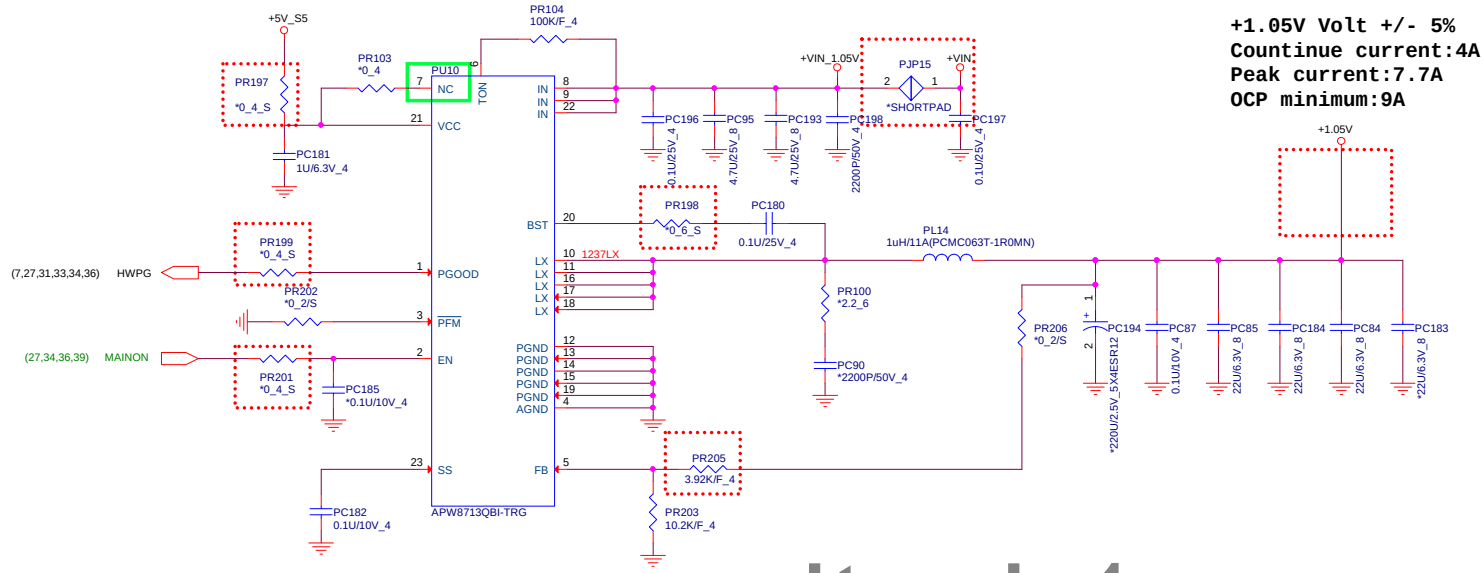
(24,25,30,31,33,34,36,37,38,39,40,41,42,51) +5V_S5
(15,29,30,31,32,33,34,37) +VIN
(2,5,10,11,40,41) +1.05V

35



+1.05V Volt +/- 5%
Countinue current:4A
Peak current:7.7A
OCP minimum:9A

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Quanta Computer Inc.		
Size: Custom	Document Number: +1.05V (APW8713)	Rev: 3B
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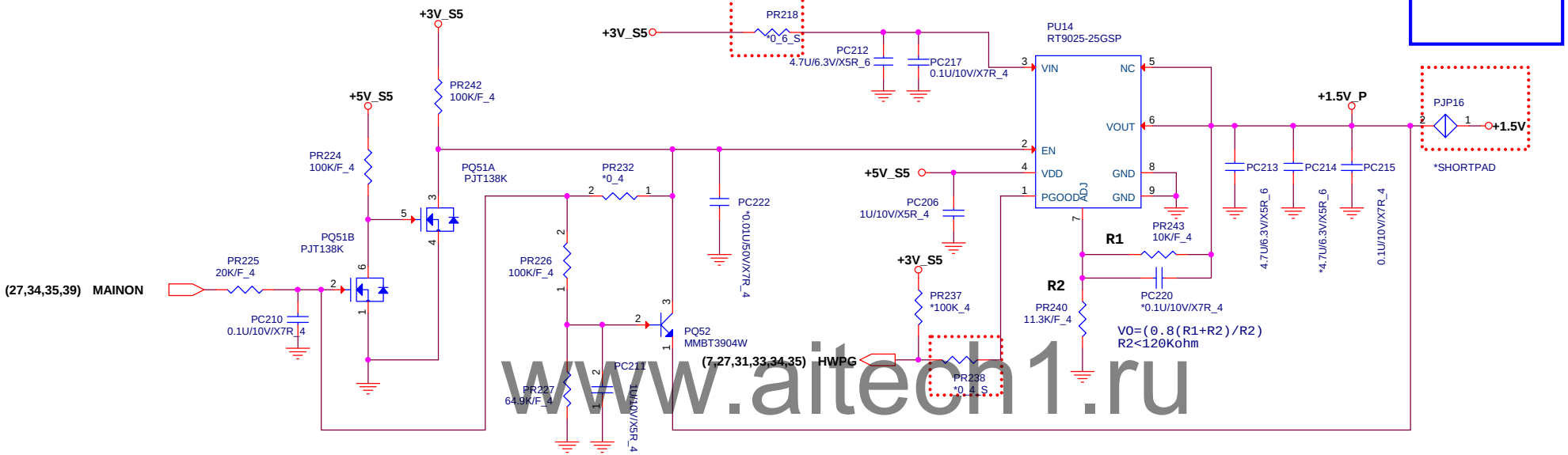
(24,25,30,31,33,34,35,37,38,39,40,41,42,51) +5V_S5
(2,7,8,9,10,11,20,23,28,30,33,37,39,40,45,51) +3V_S5
(7,8,9,11,17,18,23,41) +1.5V

+1.5V
Peak :20mA



PROJECT : NL8A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.5V (RT9025)	3B
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CPU Core : Loadline = -1.5mV/A
TDC = 33A ICCMAX=85A

OCP=120A

CPU Core : Loadline = -1.5mV/A
TDC = A ICCMAX=55A

OCP=66A

(2,4,5) VCCIO_OUT
(2,7,8,9,10,11,20,23,28,30,33,36,39,40,45,51) +3V_S5
(24,25,30,31,33,34,35,36,38,39,40,41,42,51) +5V_S5
(15,29,30,31,32,33,34,35) +VIN
(5,6,41) +VCC_CORE

3.24K for SharkBay
16.9K for CresentBay

PU6 ISL95812HRZ-T

PU7 47W@ISL6208BCRZ-T

PQ32 HP8S36TB

PQ33 HP8S36TB

PQ34 47W@HP8S36TB

PL3 0.22UH_10X10X4 Max. DCR=1.1m

PL4 0.22UH_10X10X4 Max. DCR=1.1m

PL5 0.22UH_10X10X4 Max. DCR=1.1m

PJP3 *SHORTPAD

PJP4 *SHORTPAD

PJP5 *SHORTPAD

PC144 100U/25V_105CE_f

* PR135 PLACE NEAR PL8

(Near by MOS side)

(Near by Choke side)

(Near by IC side)

C3A

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Quanta Computer Inc.

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Custom	+VCORE(ISL95812) 47W	3B
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(24,25,30,31,33,34,35,36,37,39,40,41,42,51) +5V_S5
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,39,41,43,47) +3V
(31) +VIN_NV
(42,46,47) +VGACORE

VIN2P (31)
VIN2N (31)

PU2 RT8813AGQW

PVCC UGATE1 BOOT1 PHASE1 PGOOD LGATE1 VCC/ISEN1 UGATE2 BOOT2 PHASE2 LGATE2 TALERT/ISEN2 VSNS RGND SS GND/PWM3 GND TSNS/ISEN3 TON EN PSI VID VREF REFADJ REFIN

EC-D-21
(40,47) 3V_MAIN_PWGD
(7,40,51) GFXON
(31,42) DGPU_VC_EN
(45) DGPU_PSI
(45) DGPU_PWM_VID

PR163 1_6 +5V_S5 8813PVCC PC49 0.22U/6.3V_4
PR70 1_6 +VIN_VGACORE PR68 499K/F_4 8813TON PC51 0.22U/25V_6
PR157 10K/F_4 +3V
PR76 10K/F_4 PR245 0_4/P PR246 *0_4 PD2 RB501V-40 PC58 0.22U/6.3V_4
PR168 *0_4/S 8813PSI
PR169 *0_4/S 8813VID
8813VREF PC54 0.1U/10V_4 PC60 1500P/50V_4
PR73 39K/F_4 PR72 39K/F_4 PR74 1.5K/F_4 PR172 1.5K/F_4 PR171 30K/F_4 PR170 *5.1K/F_4 8813REFADJ 8813REFIN PC55 *0.01U/16V_4
PR174 *0_4/P TP92 PR175 *10K/F_4 PQ15 *2N7002K

PR71 1_6 8813UGATE1 8813UGATE1_1
PC56 0.22U/25V_6 8813BOOT1
8813PHASE1
PQ41 TPCA8056-H PR67 16.9K/F_4 PR69 2.2_6 PC57 2200P/50V_4
PR166 10K/F_4 8813ISEN1
PC62 10U/25V_8X PC161 10U/25V_8X PC63 0.1U/25V_4 PC162 2200P/50V_4
PQ42 TPCA8064-H
PL12 0.22uH/50A
PC160 560U/2V/ESR4.5_7343 PC159 560U/2V/ESR4.5_7343
PR59 1_6 8813UGATE2 8813UGATE2_1
PC44 0.22U/25V_6 8813BOOT2
8813PHASE2
PQ37 TPCA8064-H PC151 10U/25V_8X PC38 10U/25V_8X PC37 0.1U/25V_4 PC150 2200P/50V_4
PL7 0.22uH/50A
PQ38 TPCA8056-H PR58 2.2_6 PC43 2200P/50V_4
PC59 0.1U/10V_4 PC155 560U/2V/ESR4.5_7343
PR158 *30K/F_4 PR161 10K/F_4 +5V 8813ISEN2
8813VOUT1 PC46 56P/50V_4 PC157 *100P/50V_4
8813RGN PC50 56P/50V_4
8813SS PC45 56P/50V_4
PR162 *0_4_S PR164 *0_4_S PR160 100/F_4 PR165 100/F_4 +VGACORE VGPU_CORE_SENSE (43) VSS_GPU_SENSE (43)
PR249 RC2512-R005 PR278 *0_2/S PR277 *0_2/S PC146 100U/25V_105CE_f PC145 100U/25V_105CE_f PC28 0.1U/25V_4
VIN2N VIN2P

POP Ri, Cb and NC Rh for 2phase
POP Ra and NC Rb for 2phase
Ra
Rb

+VGA_CORE
N15P-GX
Countinue current: 49A
Peak current: 76A
OCP minimum 90A

+VGA_CORE
N15E-GT
Countinue current: 76A
Peak current: 135A
OCP minimum 150A

3Phase application

PU9 RT9610BZQW
PWM EN VCC UGATE BOOT PHASE LGATE GND GND
PR193 *0_4_S 9610PWM3
PR167 *0_4 Rc
PR185 *0_4_S 9610EN
PR88 10_8 9610VCC
PC171 1U/6.3V_4
PR180 1_6 9610UGATE3 9610UGTE3_1
PD12 RB501V-40 +5V_S5
PC166 0.22U/25V_6 9610BOOT3
9610PHASE3
9610LGATE3
PQ44 TPCA8064-H
PQ43 TPCA8056-H
PR86 *2.2_6 PC66 *2200P/50V_4
PC179 10U/25V_8X PC77 10U/25V_8X PC175 0.1U/25V_4 PC72 2200P/50V_4
PL11 0.22uH/50A
PC158 330u_2.5V_7343

POP Rc for 2phase
Rg
NC Rg for 2phase
PR159 10K/F_4

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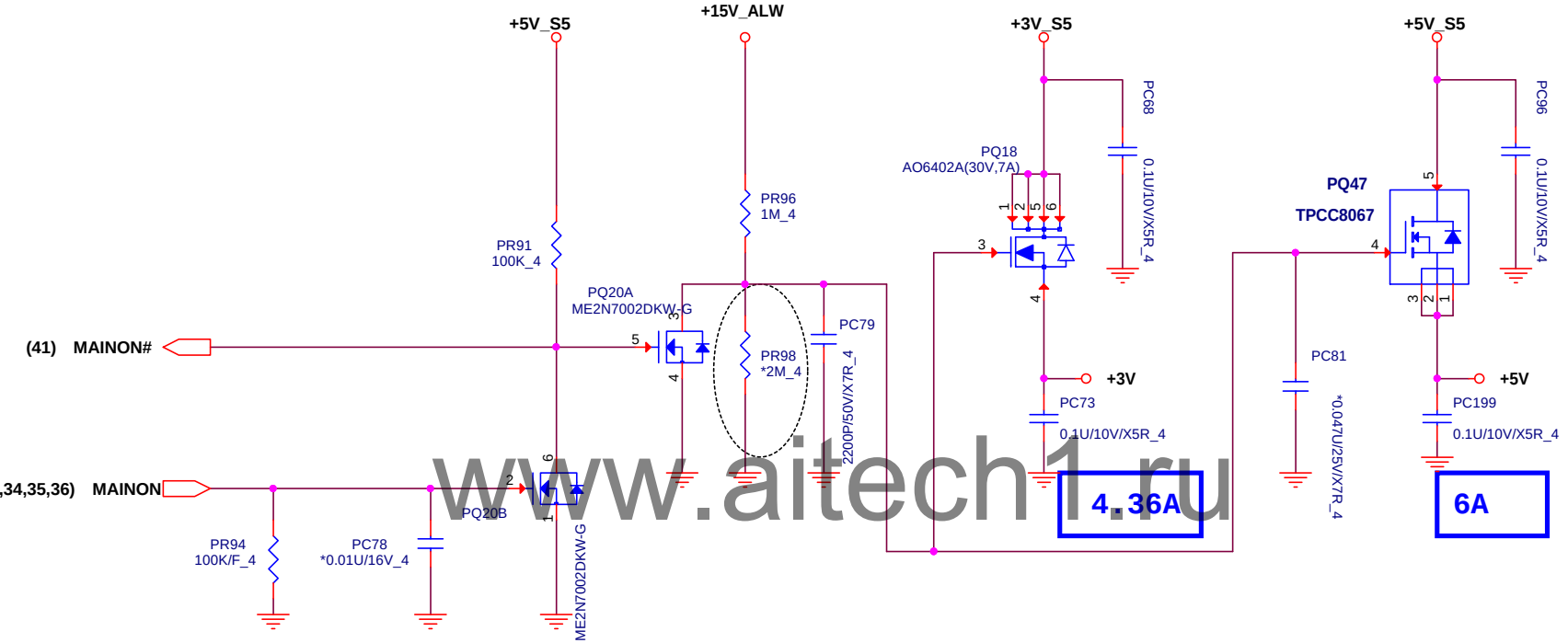
(24,25,30,31,33,34,35,36,37,38,40,41,42,51) +5V_S5
(33,40) +15V_ALW
(2,7,8,9,10,11,20,23,28,30,33,36,37,40,45,51) +3V_S5
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,41,43,47) +3V
(8,16,17,18,19,21,26,28,29,30,38,41) +5V



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Load switch	3B
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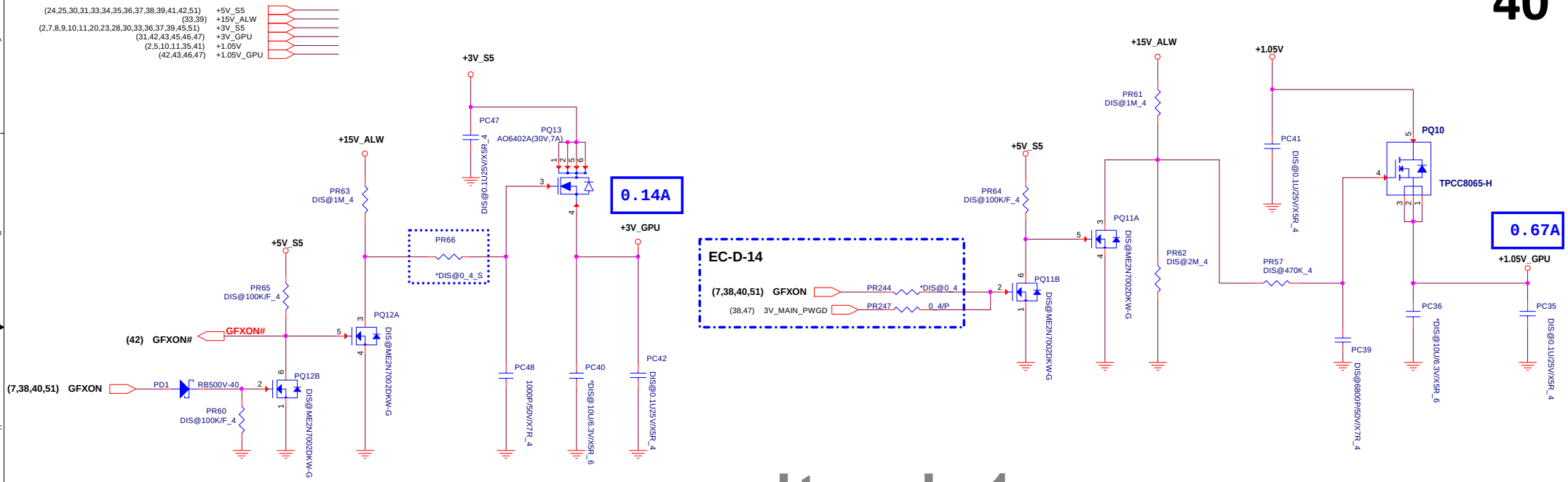

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Custom	DIS Load switch	3B
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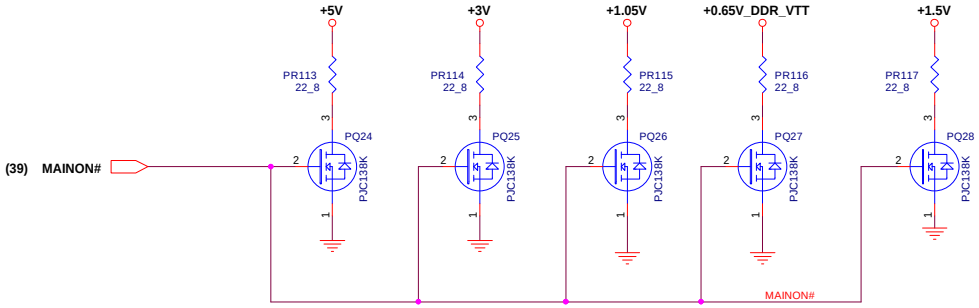
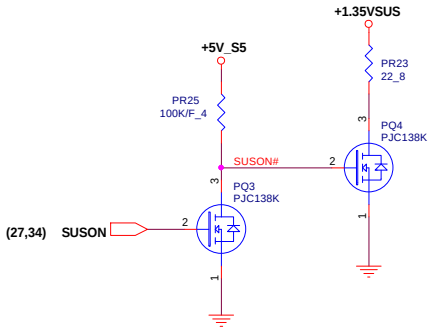
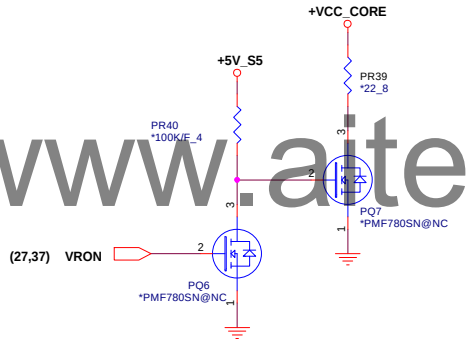
DISCHARGE

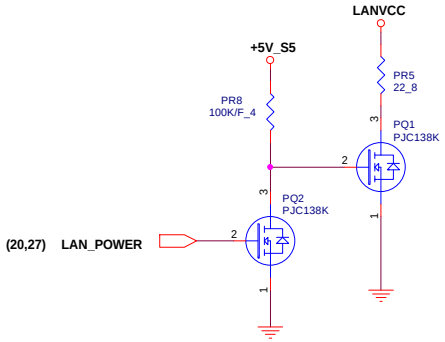
41

(8,16,17,18,19,21,26,28,29,30,38,39) +5V
(2,7,8,9,10,11,13,14,15,16,17,18,19,20,22,25,26,27,28,30,38,39,43,47) +3V
(2,5,10,11,35,40) +1.05V
(13,14,34) +0.65V_DDR_VTT
(7,8,9,11,17,18,23,36) +1.5V
(2,5,13,14,34) +1.35VSUS
(24,25,30,31,33,34,35,36,37,38,39,40,42,51) +5V_S5
(5,6,37) +VCC_CORE
(20) LANVCC









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Custom	Discharge	3B
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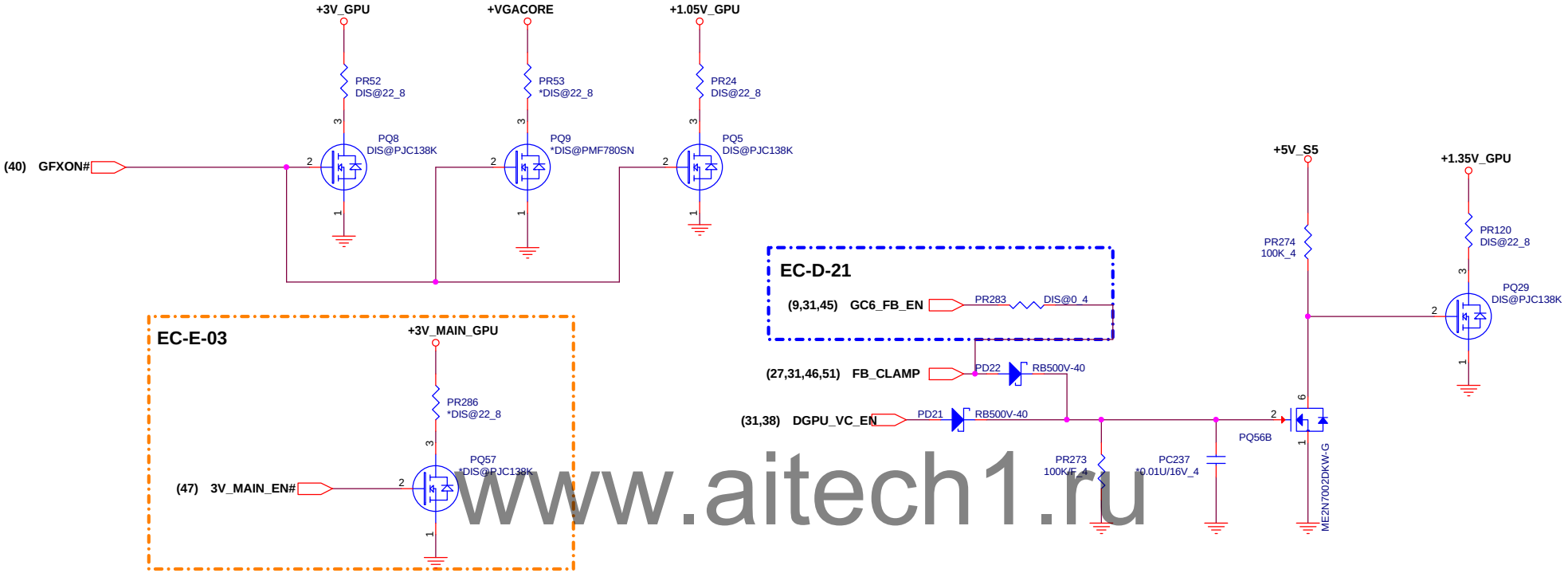
Discrete only

(31,40,43,45,46,47) +3V_GPU
(38,46,47) +VGACORE
(40,43,46,47) +1.05V_GPU
(31,43,44,46,47,48,49,50) +1.35V_GPU
(43,45,46,47) +3V_MAIN_GPU



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Size	Document Number	Rev
Custom	Discrete Discharge	3B
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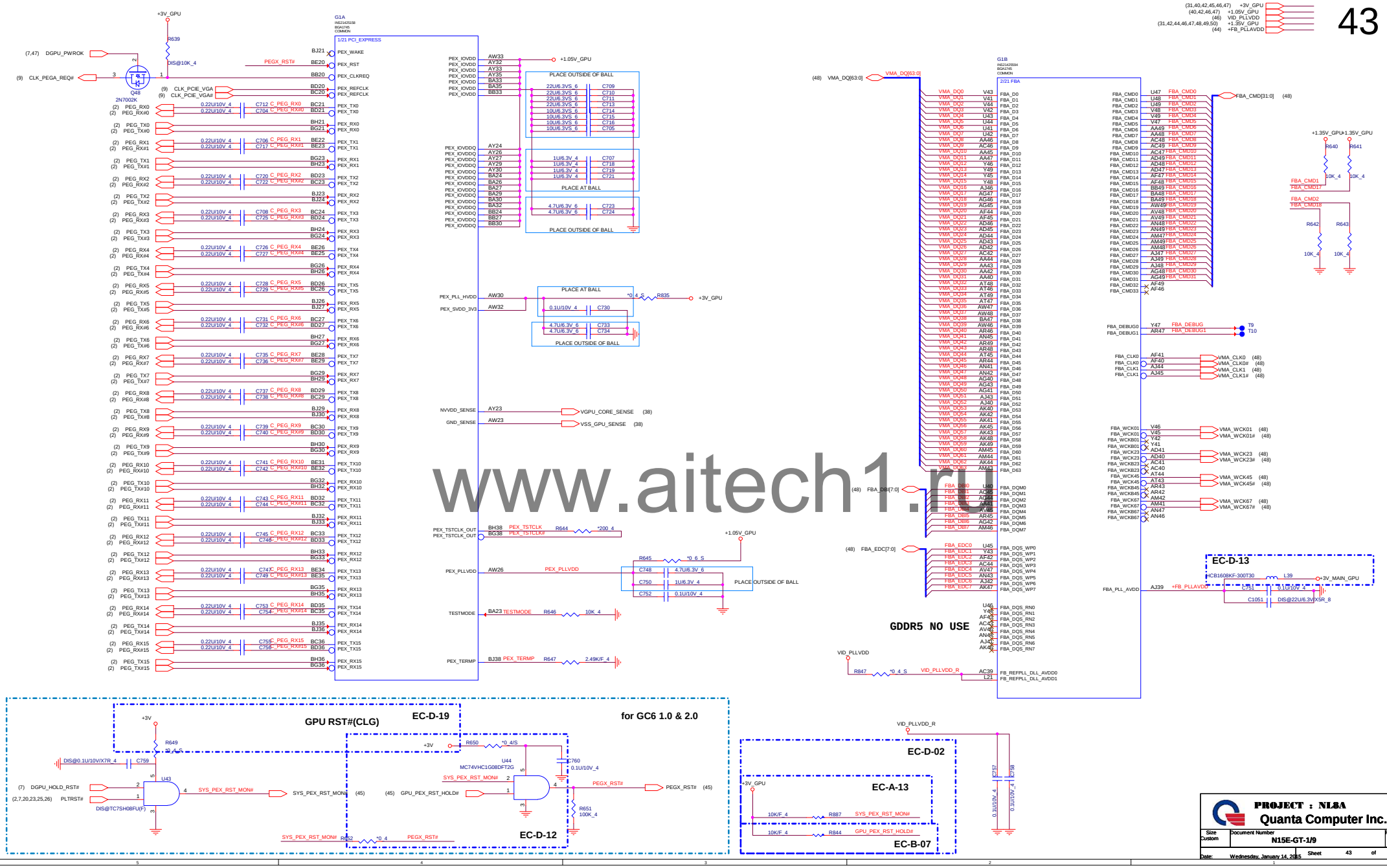
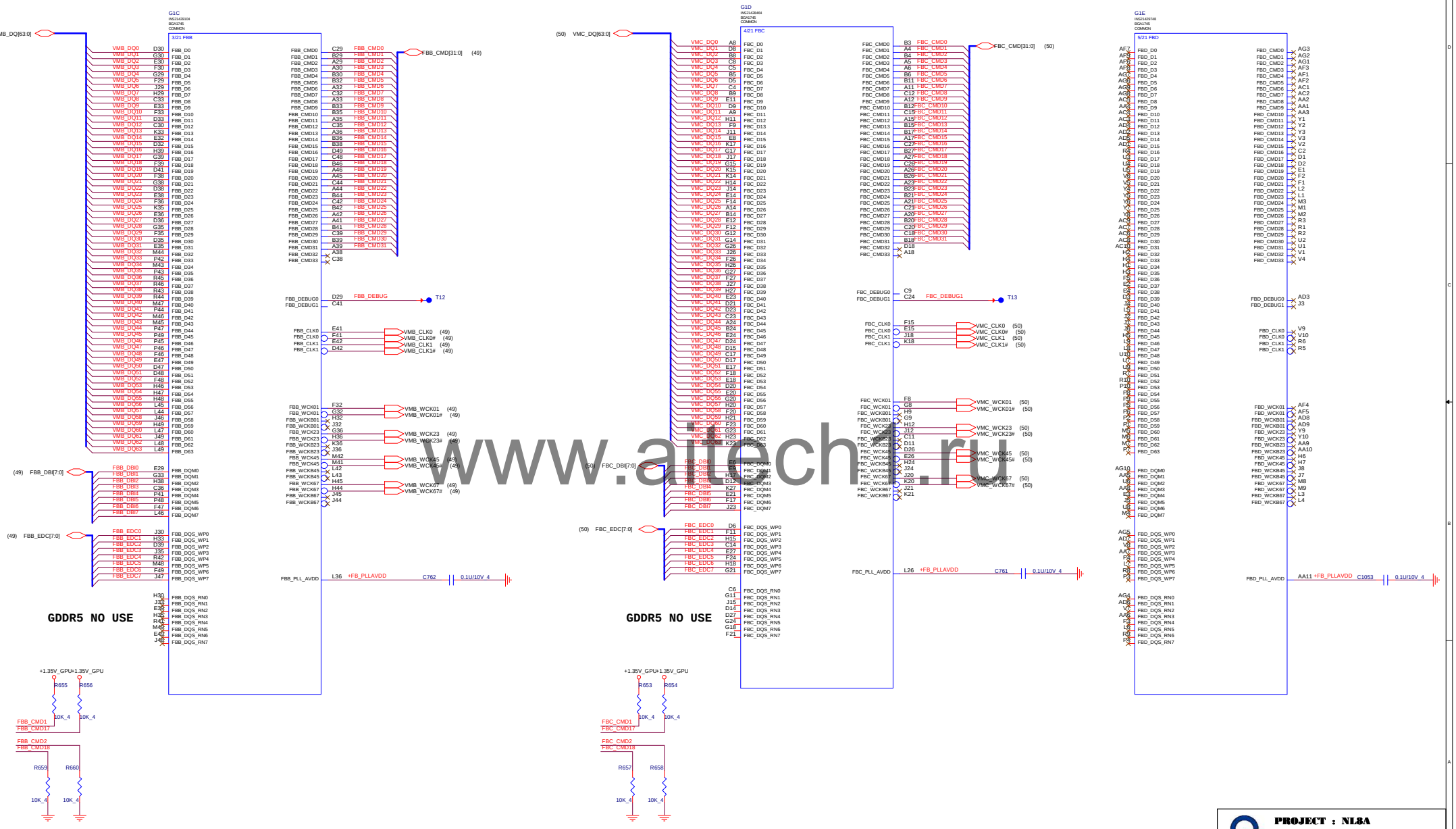


(31,42,43,46,47,48,49,50) +1.35V_GPU
(43) +FB_PLLAVDD



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Size	Document Number	Rev
Custom	N15E-GT-2/9	3B
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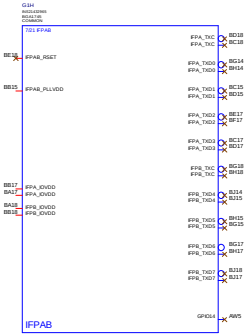
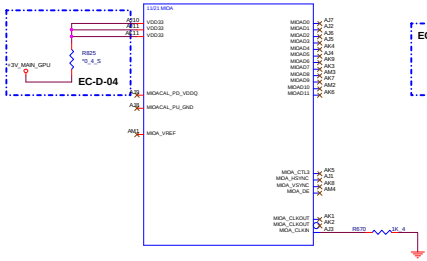
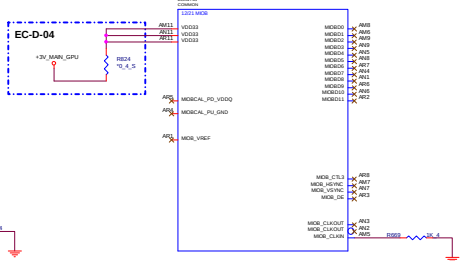
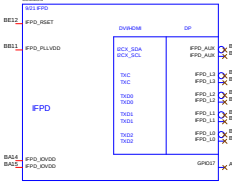
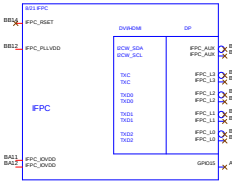










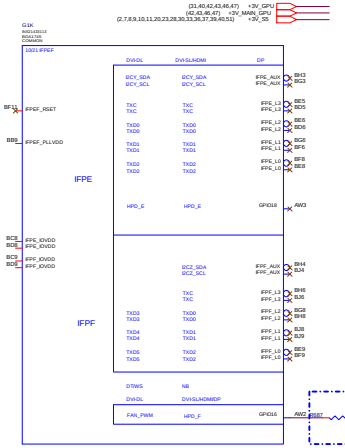


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-3 and Table15-4 contain mapping tables for the Multi-Level Strapping Modes.

N15E-GX/GT GDDR5 MEMORY RVL

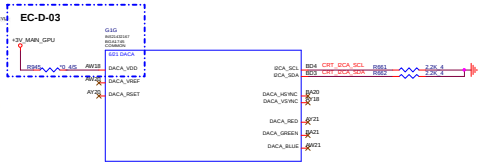
NVIDIA recommends the following GDDR5 memories for use in conjunction with notebook designs using N15E-GX/GT GPU.

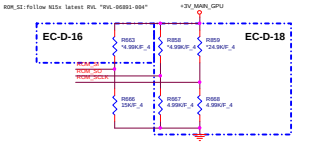
Note: For N15E-GX/-GT, the maximum allowable memory case temperature is 115 °C, as these are our highest end flagship GPUs.

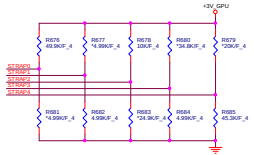
Table 12. N15E-GX/GT GDDR5 Recommended Memories

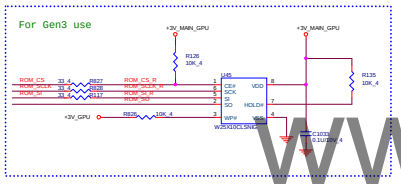
Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Clk Grade(MHz)	Memory Data Code Minimum	Status
GDDR5	1.35V/ 1.35V	128Mx16	Hynix	H5GQ2H24AFR-R0C	A-die	0x6	2500	N/A	Production candidate
			Samsung	K4G03325FD-FC03	D-die	0x7	2500	N/A	Production candidate
		256Mx16	Hynix	H5GC4H24MFR-T2C	M-die	0x1	2500	N/A	Production candidate
			Micron	EDW4032BABG-60-F	A-die	0x3	2500	N/A	Production candidate
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production candidate

256M x16	H5GC4H24MFR-T2C	AKG5PWUTW06
256M x16	K4G41325FC-HC03	AKG5PGDT500



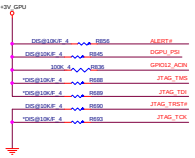


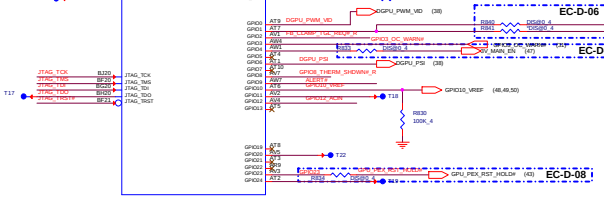


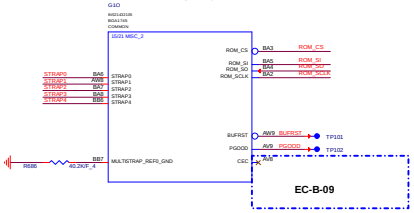


Default: GDDRS Hynix 2G VRAM (for NL8)

Memory Size	Vendor	P/N	Mfr. P/N	ROM_SI	
128M x 16	Hynix (1.35V)	AKG5MWUTW23	H5GC2H24BFR-T2C	0001 (0x1)	10K PD
256M x 16	Hynix (1.35V)	AKG5MWUTW06	H5GC4H24MFR-T2C	0010 (0x2)	15K PD
128M x 16	Samsung (1.35V)	AKG5MWDTS02	K4G20325FD-FC03	0000 (0x0)	4.99K PD
256M x 16	Samsung (1.35V)	AKG5PGDTS00	K4G41325FC-HC03	0011 (0x3)	20K PD
128M x 16	Micro (1.35V)	AKG5MWBTL03	EDW2032BBBG-6A-F-R		30.1K PD







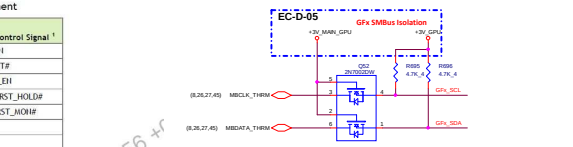


Table 1. N15E-GX / -GT GC6 Pin Assignment

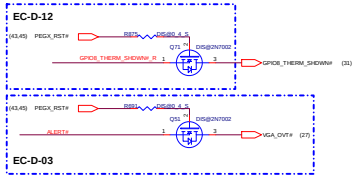
GPIO/ Power Rail	GC6 1.0 Control Signal	GC6 2.0 Control Signal [1]
GPIO1	FB_CLAMP_MON#	GC6_FB_EN
GPIO2	FBCLAMP_TGL_REQ#	GPU_EVENT#
GPIO4	Reserve	3V3_MAIN_EN
GPIO23	Reserve	GPU_PEX_RST_HOLD#
CEC	HC	SYS_PEX_RST_MON#
PEX_PLL_HVDD	VDD33	3V3_AON
PEX_SVDD_3V3	VDD33	3V3_AON
3V3MI5C	VDD33	3V3_AON

Note:

1. All GPIO, I2CA/B/C/S, DAC_H/V_SYNC, PCIe Reset, CLKREQ#, XTAL, and JTAG signals, when pulled-up, should be connected to the 3V3_AON power rail for GC6 2.0.

Table 12-2. GB3-256 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO1	FB_CLAMP_MON#	I	FB clamp monitor	
GPIO2	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	10K pull-up to system 3.3V
GPIO3	OC_WARN#	I	Over current interrupt for IPC	10K pull-up
GPIO4	Reserved			
GPIO5	Reserved			
GPIO6	PSI	O	Phase Shedding	PSI: 10k pull-up to enable two phase.
GPIO7	LCD_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	
GPIO16	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or IFPB	
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	



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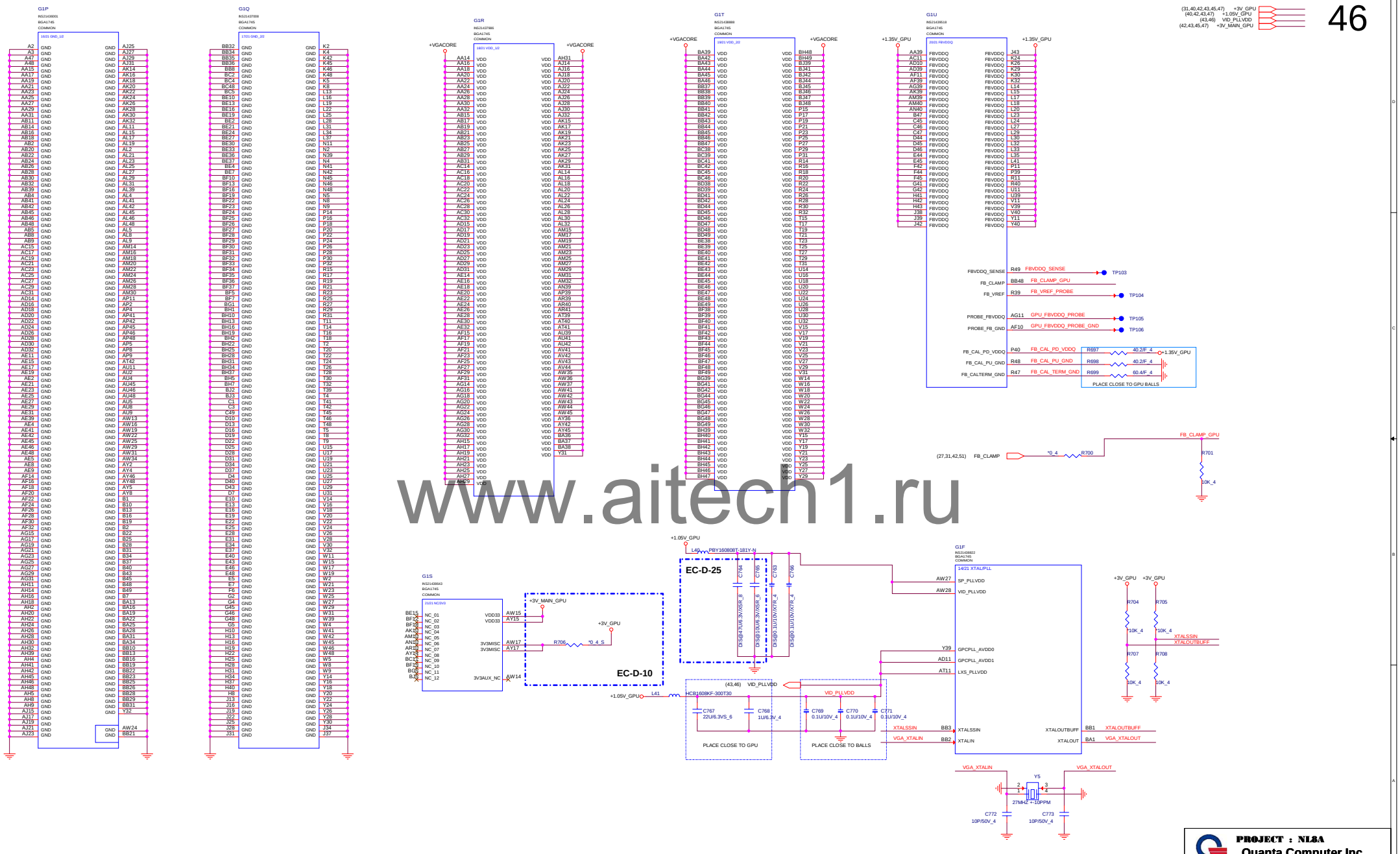

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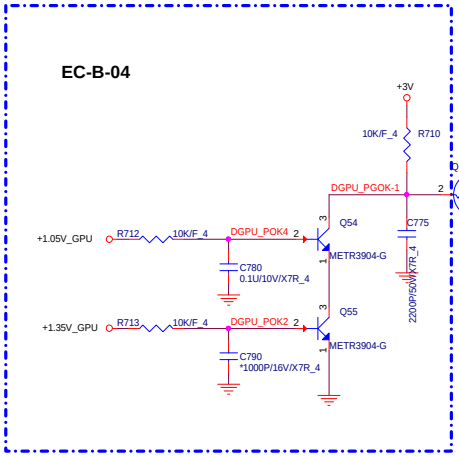

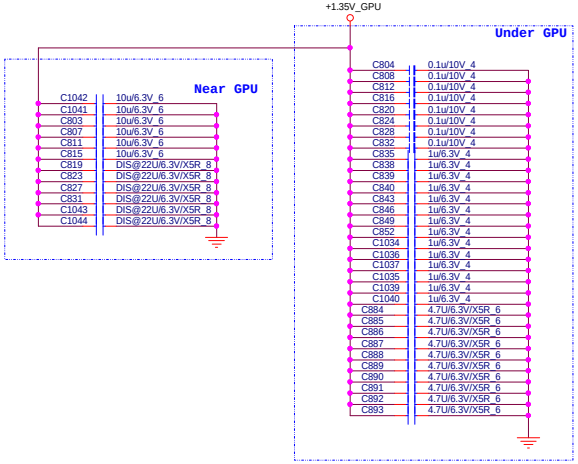

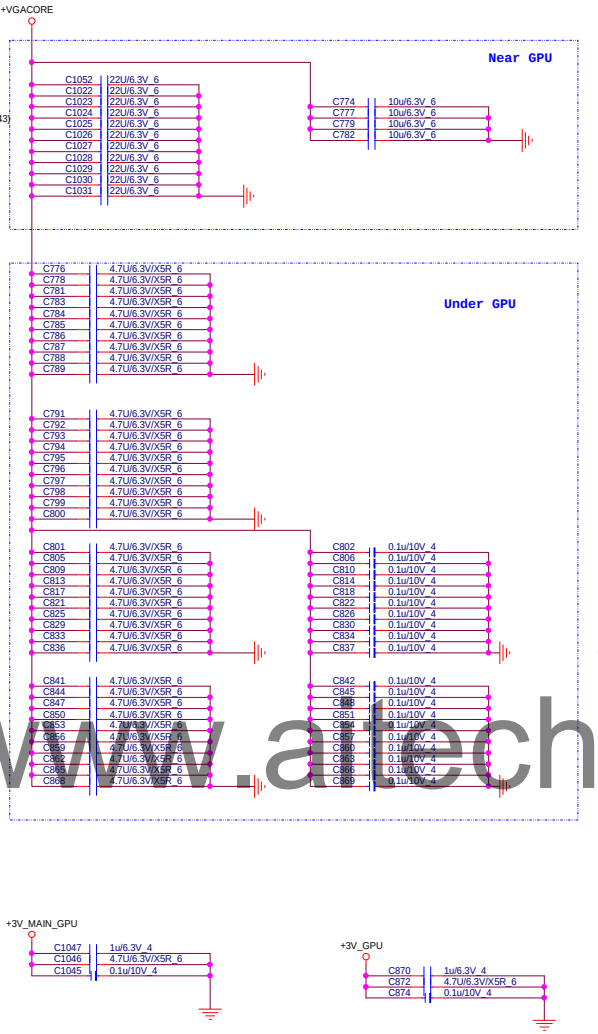

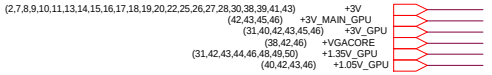

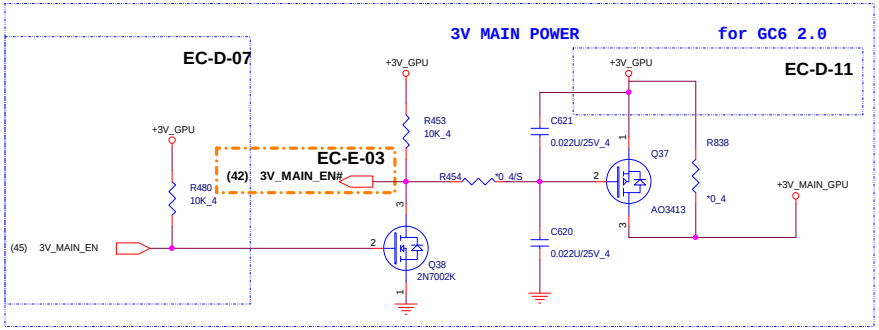

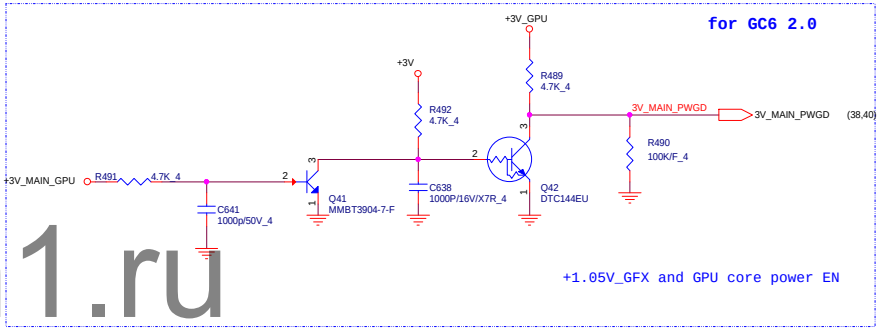

for meet Power down sequence for +3V_GFX

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CHANNEL A: 2G/4G GDDR5

(43) VMA_DQ[63..0] VMA_DQ[63..0]
(43) FBA_CMD[31:0] FBA_DB[7..0]
(43) FBA_DBI[7..0]
(43) FBA_EDC[7..0] FBA_EDC[7..0]

(31,42,43,44,46,47,49,50) +1.35V_GPU

Channel 0 <0-31>
MF=0 Non-mirrored

QD16~23

QD0~7

VRAM1

VREFD_VMA1 0.4MM=16mils

VREFC_VMA1 0.4MM=16mils

Channel 0 <0-31>
MF=1 Mirrored

QD8~15

QD24~31

VRAM2

VREFD_VMA1 0.4MM=16mils

VREFC_VMA1 0.4MM=16mils

Channel 1 <32-63>
MF=0 Non-mirrored

QD48~55

QD32~39

VRAM3

VREFD_VMA2 0.4MM=16mils

VREFC_VMA2 0.4MM=16mils

Channel 1 <32-63>
MF=1 Mirrored

QD40~47

QD56~63

VRAM4

VREFD_VMA2 0.4MM=16mils

VREFC_VMA2 0.4MM=16mils

Table 7-5. GDDR5 Mode F Mapping

GB3-256	CA*	GB3-256	Channel 1 32..63
CMD0	CA*	CMD16	CA*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0		
CMD35	DEBUG1		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

(44) VMB_DQ[63..0] VMB_DQ[63..0]
(44) FBB_CMD[31:0] FBB_CMD[31:0]
(44) FBB_DBI[7..0] FBB_DBI[7..0]
(44) FBB_EDC[7..0] FBB_EDC[7..0]

(31,42,43,44,46,47,48,50) +1.35V_GPU

Channel 0 <0-31>
MF=0 Non-mirrored
QD16~23
QD0~7

Channel 0 <32-63>
MF=1 Mirrored
QD8~15
QD24~31

Channel 1 <0-31>
MF=0 Non-mirrored
QD48~55
QD32~39

Channel 1 <32-63>
MF=1 Mirrored
QD40~47
QD56~63

Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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(44) VMC_DQ[63..0] — VMC_DQ[63..0]
(44) FBC_CMD[31:0]
(44) FBC_DBI[7..0] — FBC_DBI[7..0]
(44) FBC_EDC[7..0] — FBC_EDC[7..0]

(31,42,43,44,46,47,48,49) +1.35V_GPU

Channel 0 <0-31>
MF=0 Non-mirrored
QD16~23
QD0~7

Channel 0 <32-63>
MF=1 Mirrored
QD8~15
QD24~31

Channel 1 <0-31>
MF=0 Non-mirrored
QD48~55
QD32~39

Channel 1 <32-63>
MF=1 Mirrored
QD40~47
QD56~63

VRAM9 — VRAM10 — VRAM11 — VRAM12

Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CA5*	CMD16	CA5*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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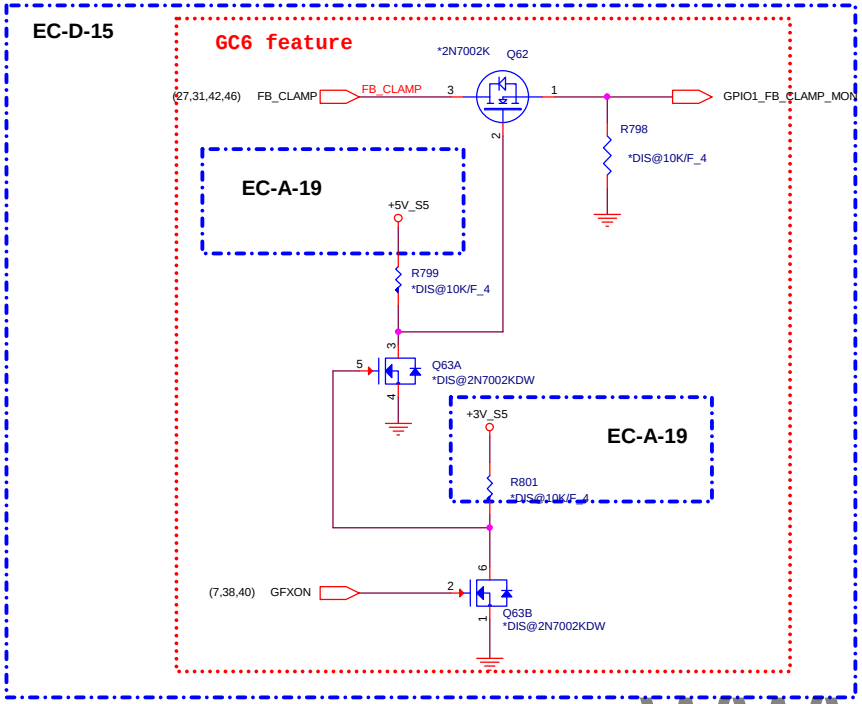

Power rail	State in GC6
3V3_AON	On
3V3_MAIN	Off
PEX_1.05V	Off
NVVDD	Off
FBVDD/Q	On

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2013

SDV~SIV

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	21	02/19	CN20	HDD pin define change.
EC-A-02	26	02/19	Q67	change to Q66A(delete Q67).
EC-A-03	28	02/19	R881,R882,R883	add for current limit
EC-A-04	18,19	02/19	C1058,C1059,C458,R884,C1060	co-lay line and mono-out for subwoofer
EC-A-05	19	02/20	U21	change to AND GATE
EC-A-06	11	02/20	L5	depop
EC-A-07	7	02/20	R862,R863,R536,R548	R862,R863,R536,R548 change to 8.2K
EC-A-08	18	02/20	Q47	Q47 chnage to BAM34090009 for SPDIF LED always tune on issue
EC-A-09	7	02/20	R602	R602 change to 1K to follow CRB
EC-A-10	8	02/20	R526	POP
EC-A-11	48	02/21	R885	reserve 10K for GC6_FB_EN
EC-A-12	48	02/21	R886	reserve R886 for GC6 2.0 GPU_EVENT need pull up to 3V3_AON
EC-A-13	46	02/21	R887	reserve R887 for GC6 2.0 SYS_PEX_RST_MON# need pull up to 3V3_AON
EC-A-14	7,27	02/24	R880	change R880 to 100K pull low and GFXON change from EC to PCH(for GC6 2.0)
EC-A-15	48	02/26	R888,R889	reserve to follow DG but CRB pull low
EC-A-16	28	02/27	R874	change net form KB_LIGHT to KB_LIGHT_P due to same net name as EC control
EC-A-17	24,25	02/27		change U3B(real side) form MB to FB
EC-A-18	9	02/27	R598	add CLKREQ# for card reader and R598 change to pull up
EC-A-19	54	02/27		change power rail
EC-A-20	28	03/04		move LID function to PWR/B

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2014

SIV~SIT

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-B-01	17	04/01		change HDMI solution to support 4K*2K
EC-B-02	10	04/01	R320	add R320 to avoid GPIO float.
EC-B-03	20	04/01	R52	change to +3V for lan wake issue
EC-B-04	50	04/01	R713,R712,C790,C780,R710,C775	change DGPU PWR OK power sequence
EC-B-05	7	04/02	R281	ACPI for GPU(improve perf. under DC mode)
EC-B-06	20	04/03	C31,C543	C31,C543 change to 8.2p for X'tral report
EC-B-07	46	04/03	R844	GPIO23 for GC6 1.0 just only reserve
EC-B-08	47	04/07		delete T11/T14 due to located on no probe area
EC-B-09	48	04/07		change SYS_PEX_RST_MON# from CEC to GPIO16
EC-B-10	18,19	04/07	D27,D28,D29,D30,D31,R939	for SUBWOOFER pop noise issue
EC-B-11	22	04/08		SSD_DEVSLP chnage to pin44
EC-B-12	28	04/09		change CN5.9 to 3VPCU(user define key)
EC-B-13	19	04/11	C1081,C1082	add C1081 for subwoofer RC filter & reserve C1082 for pi filter
EC-B-14	25	04/11	CN14	change CN14 pin define
EC-B-15	18	04/11	C1058,C1059	change to 10u
EC-B-16	18	04/17	R345,R346	change to 47K for PC beep sound

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SIT~SVT

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-C-01	27	05/19	SW1	remove form SVT stage
EC-C-02	15	05/19		CCD pin define change
EC-C-03	22	05/19	CN8,CN18	pin43 change to NA
EC-C-04	19	05/22	R943,R944	reserve for POP noise
EC-C-05	48	05/28	R669,R670	remove for MIO interface no support

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SIT~SVT

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-D-01	09,10	9/16	R870,R871;R538,R539,R575,R594,R554,R562	GC6 2.0;board ID;
EC-D-02	43	9/15	R887	reserve for GPIO pull up +3V_GPU(GC6 2.0)
EC-D-03	45	9/15	DACA_VDD, R945	reserve for N16E add +3V_MAIN_GPU pin(thermal detect)
EC-D-04	45	9/15	R824, R825 (short)	+3V-GPU change to +3V_MAIN_GPU (GC6 2.0)
EC-D-05	45	9/15	GFx_SCL, GFx_SDA	+3V_MAIN_GPU change to +3V_GPU (GC6 2.0)
EC-D-06	45	9/15	R840, R841, R885	reserve to GC6 2.0
EC-D-07	45, 47	9/15	R833, R480	reserve to GC6 2.0; pull up +3V_GPU
EC-D-08	43, 45	9/15	R834, R844	reserve to GC6 2.0; pull up +3V_GPU
EC-D-09	45	9/15	R869	+3V_MAIN_GPU change to +3V_GPU (GC6 2.0)
EC-D-10	46	9/15	VDD33, 3V3MISC	+3V-GPU change to +3V_MAIN_GPU; +3V_MAIN_GPU change to +3V_GPU (GC6 2.0)
EC-D-11	47	9/15,9/17	C621	+3V_GPU change to +3V; change back +3V_GPU
EC-D-12	43, 45	9/15	R650,R652,U44,C760,R687,R875,Q71,R691,Q51	reserve to GC6 2.0
EC-D-13	43	9/15	L39	+3V-GPU change to +3V_MAIN_GPU (GC6 2.0)
EC-D-14	40	9/15	PR244, PR247	GFXON change to 3V_MAIN_PWGD (GC6 2.0)
EC-D-15	51	9/15	R798, R799, R801, Q62, Q63	GC6 feature remove
EC-D-16	45	9/15	R676	change to 49.9K
EC-D-17	45	9/15	R864,Q69,R886, R865,R831,R832	reserve to FB_CLAMP_TGL_REQ#_R(GC6 2.0)
EC-D-18	45	9/16	R667,R668,R868,R869	multi-level mode strapping

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SIT~SVT

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-D-19	43	9/17	U43,U44	+3V_GPU change to +3V(Nelson)
EC-D-20	45	9/17	Q52 pin5	+3V_GPU change to +3V_MAIN_GPU(Nelson)
EC-D-20	38	9/17	PR245,PR246	GFXON change to +3V_MAIN_PWGD
EC-D-21	31, 42	9/17	PR266,PR283	GC6_FB_EN derive 1.35_GPU
EC-D-22	27, 46	9/17	R866, R700	FB_CLAMP discable
EC-D-23	5,7,11	9/18	R946, R947, R948, C1084	Haswell & Broadwell Compatibility Considerations
EC-D-24	7	9/18	R338	Haswell & Broadwell Compatibility Considerations
EC-D-25	46	10/06	C764, C765	VID_PLLVDD power rail filtering combined form Albert

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SIT~MV

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-E-01	10	11/12	R949	Add GPIO35 for board ID
EC-E-02	27,28	11/12	CN31,R950,R951	Add Breathe LED function
EC-E-03	42,47	11/12	PQ57,PR286	Add +3V_MAIN_GPU discharger circuite
	29	11/18	H34	GND pad remove for new 4 pin connector
EC-E-04	28	11/19	C1085,C1086,C1087,C1088	Add Breathe LED function EMI ESD part

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SIT~MV

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-F-01	27,28	12/09	CN32,C1089~C1097,U15	add power button conn for NL9
EC-F-02	27,28	12/09	CN33,R952,R953,C1098~C1103,U15	add touch PAD WHITE/RED LED for NL9
EC-F-03	8,27	01/13	Q72, R954; R867 no stuff	add EC RTC RST for system can't power on untill remove RTC issue

PROJECT : NL8A

Quanta Computer Inc.

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Custom	EC list-3	3B
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